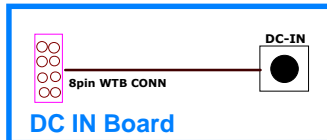
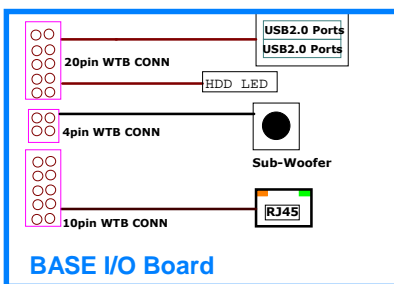
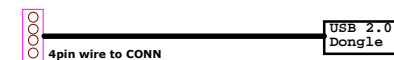
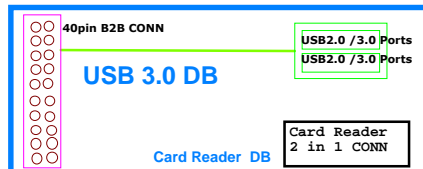
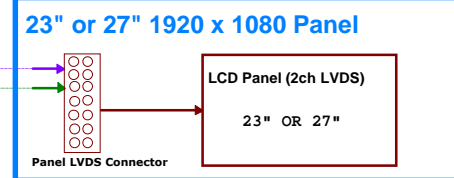
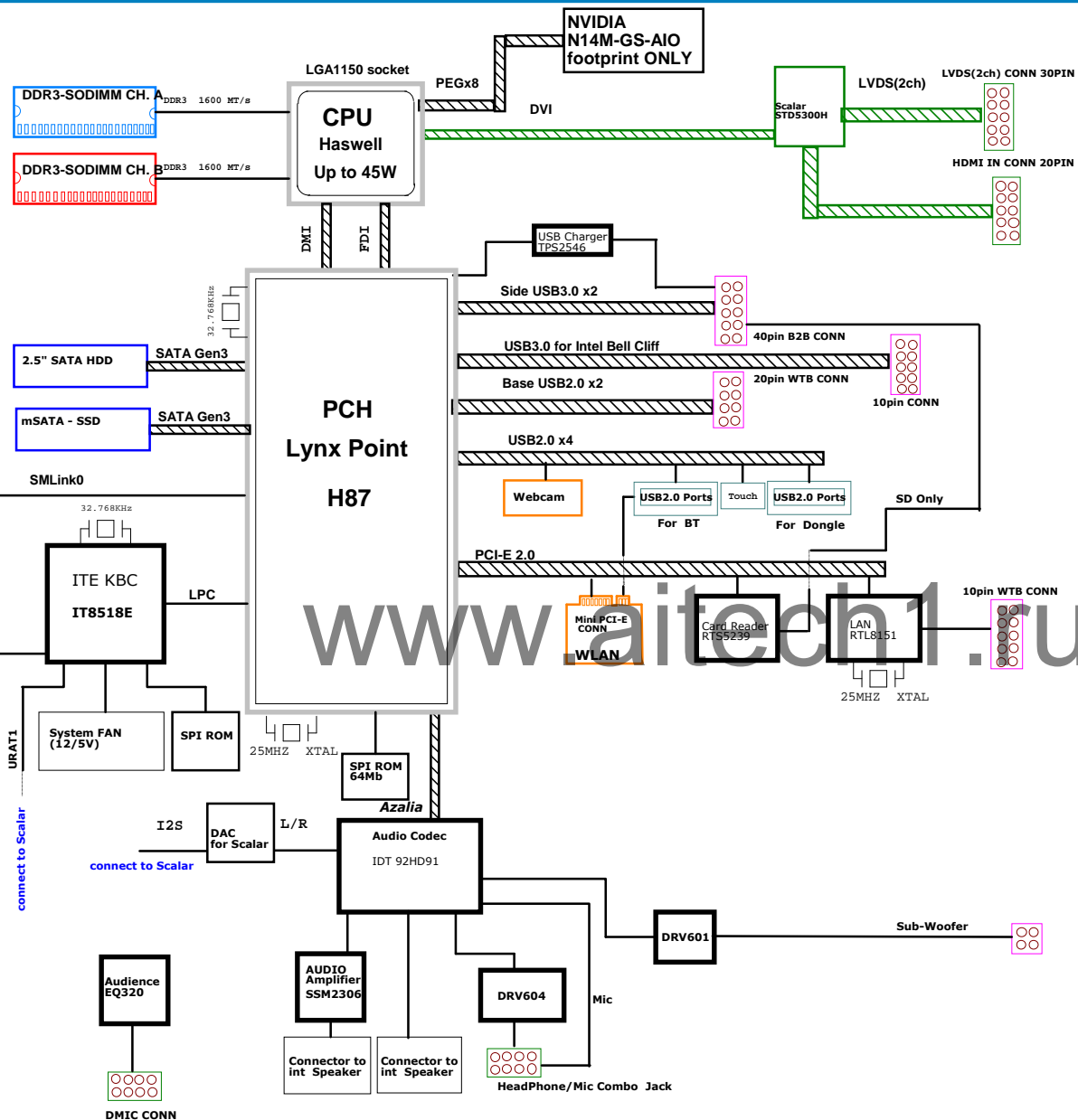


HP ELM System Block Diagram

1

M/B

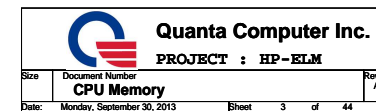


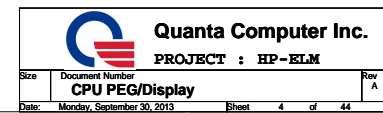
PWR BTN

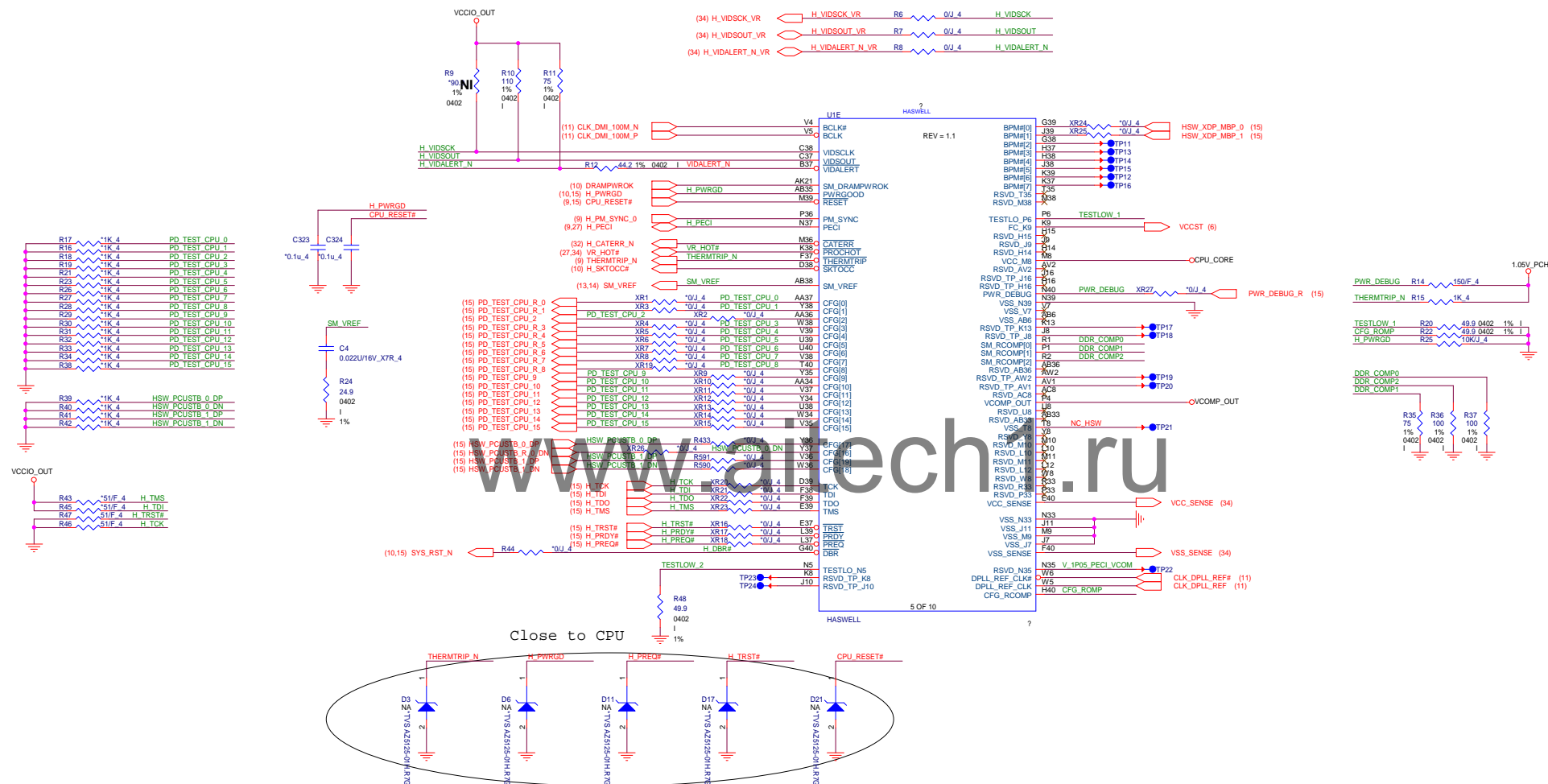
DMIC UPWARD

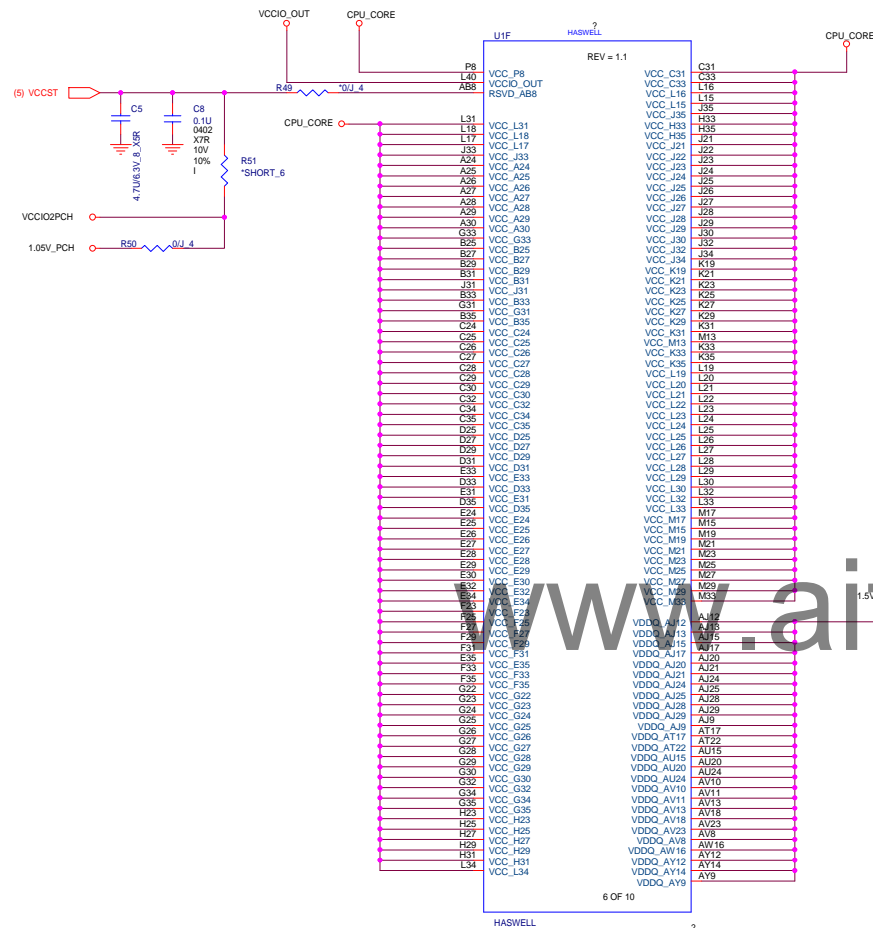
DMIC BACKWARD

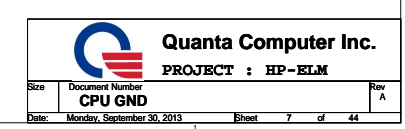
CONFIDENTIAL

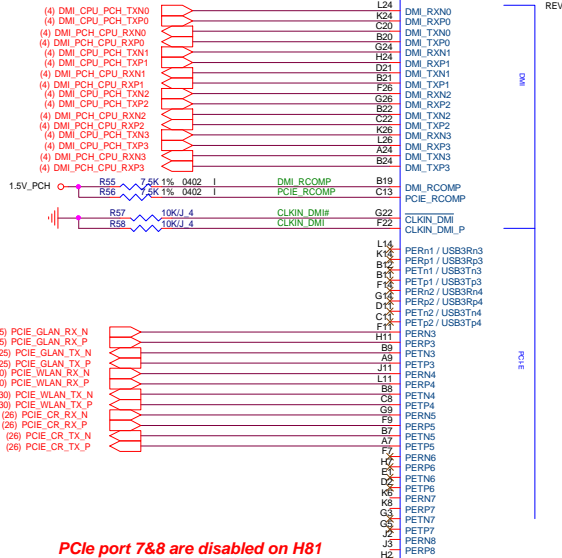
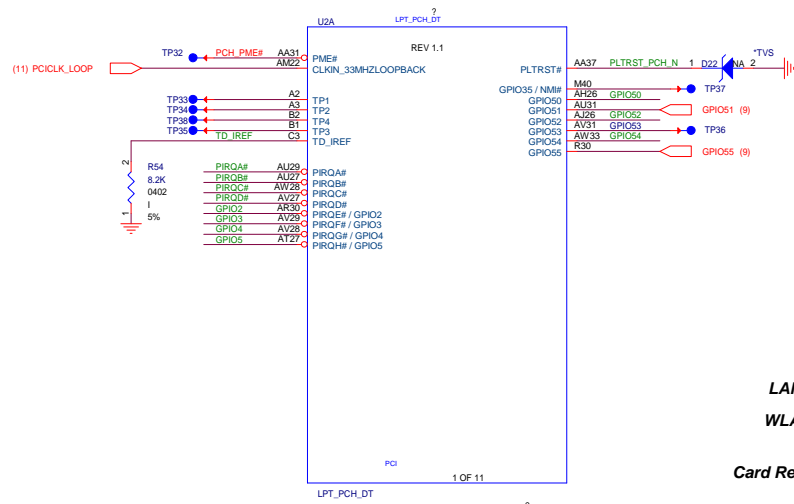






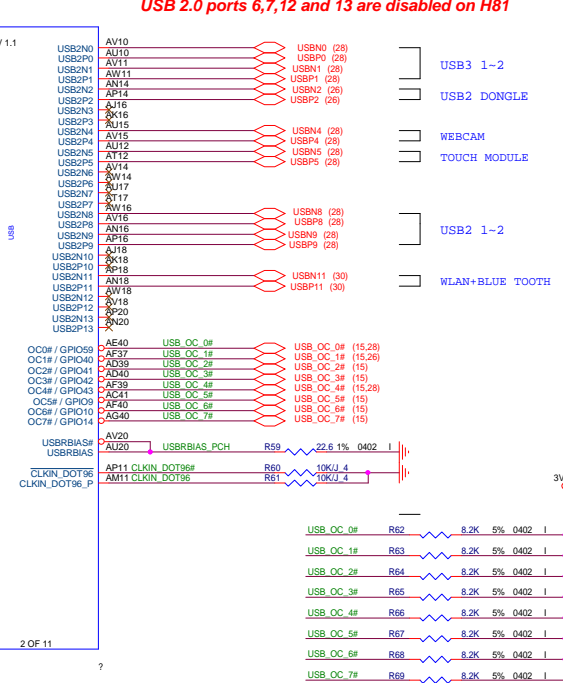




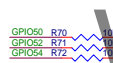
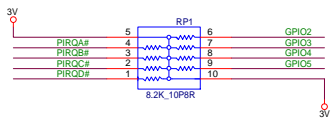


LAN
WLAN
Card Reader

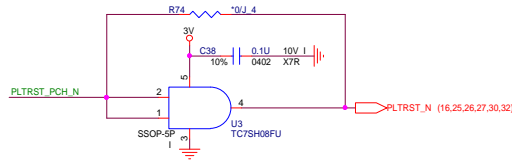
PCIe port 7&8 are disabled on H81



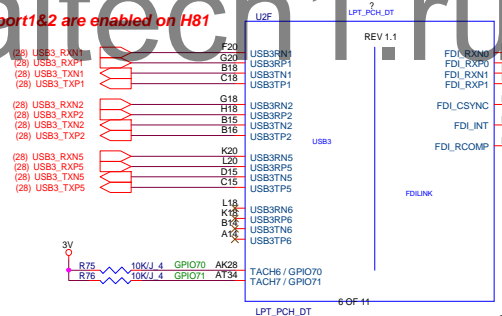
PCI PULL-UPS



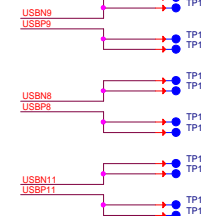
PCH PLTRST

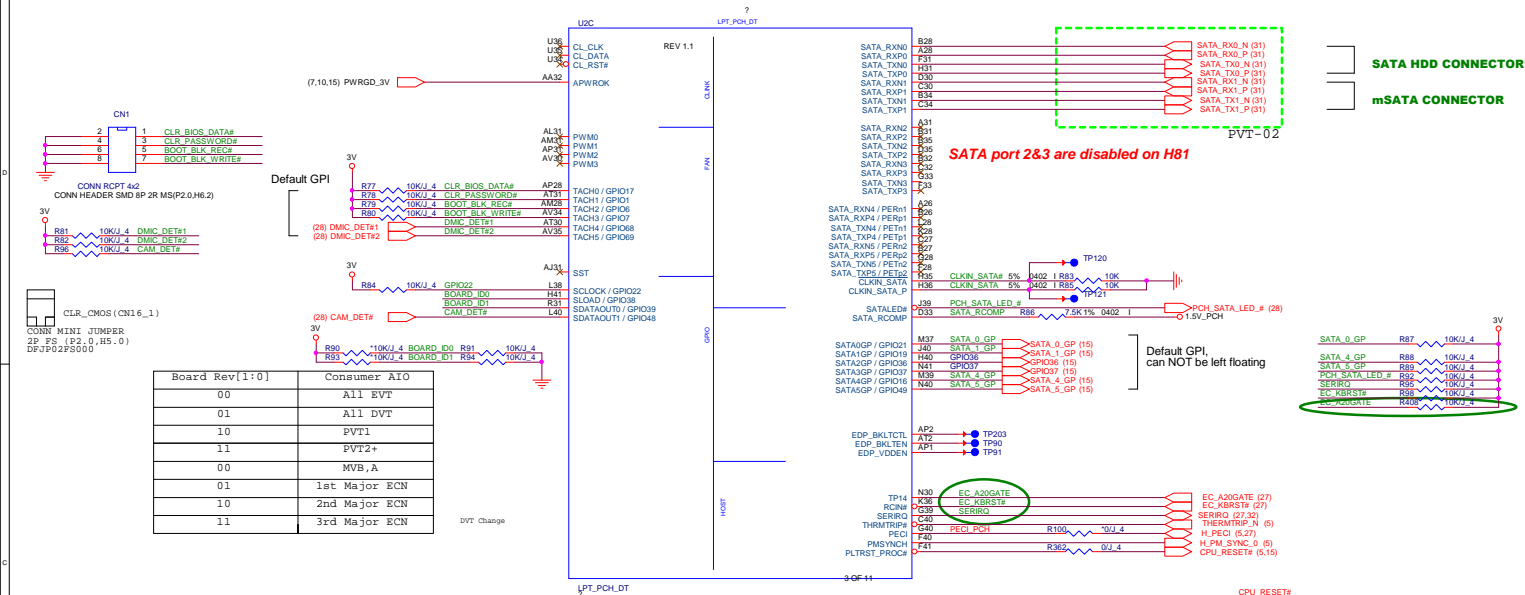


Add for ELM bell cliff
8/14















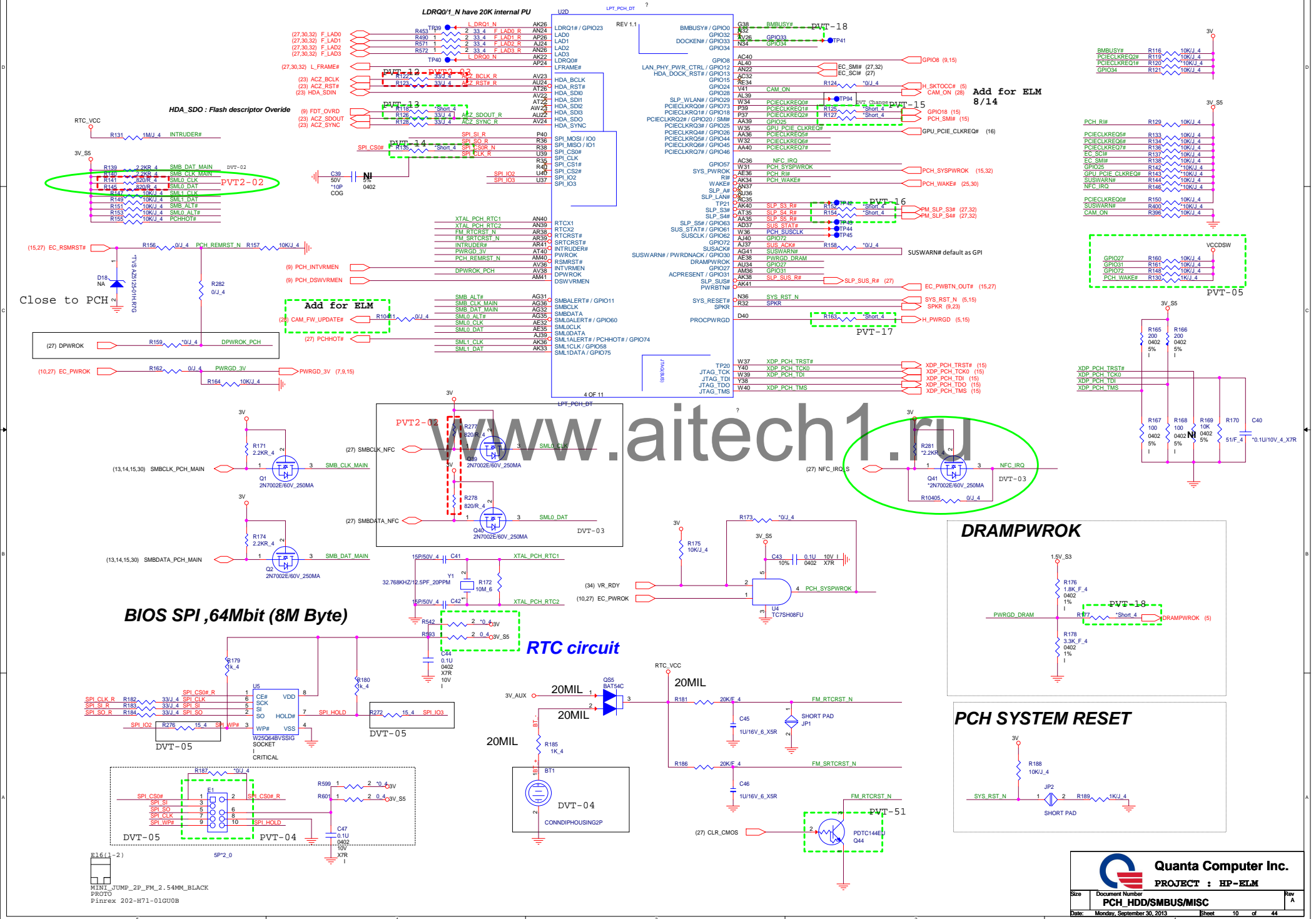
Only USB3.0 port1&2 are enabled on H81

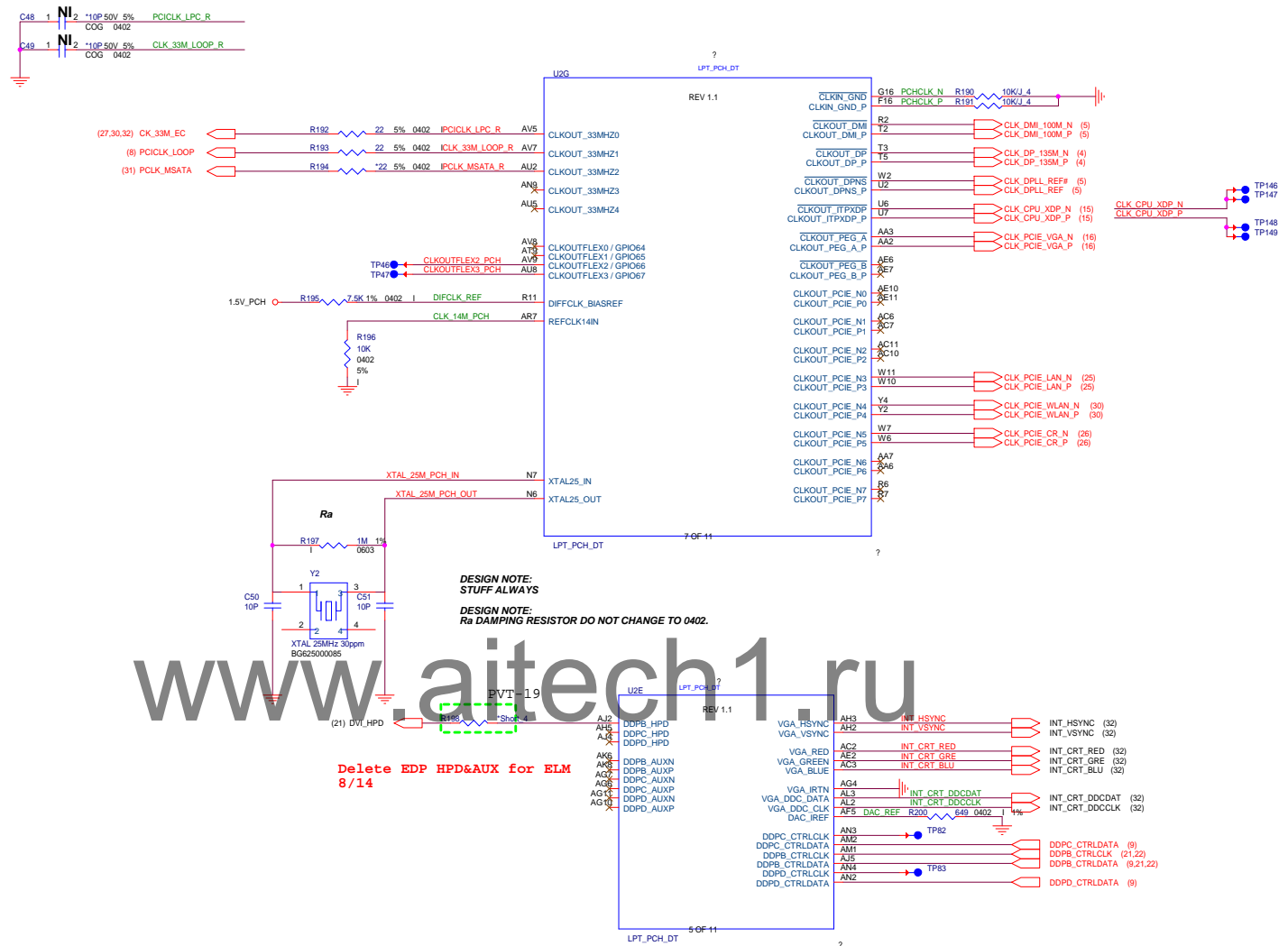


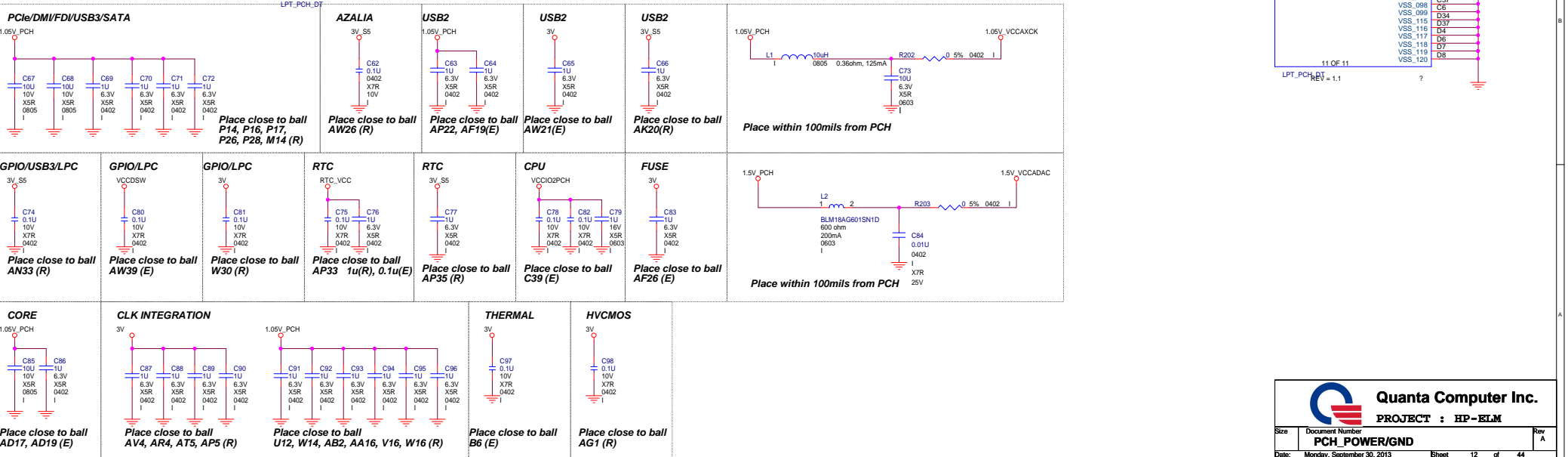
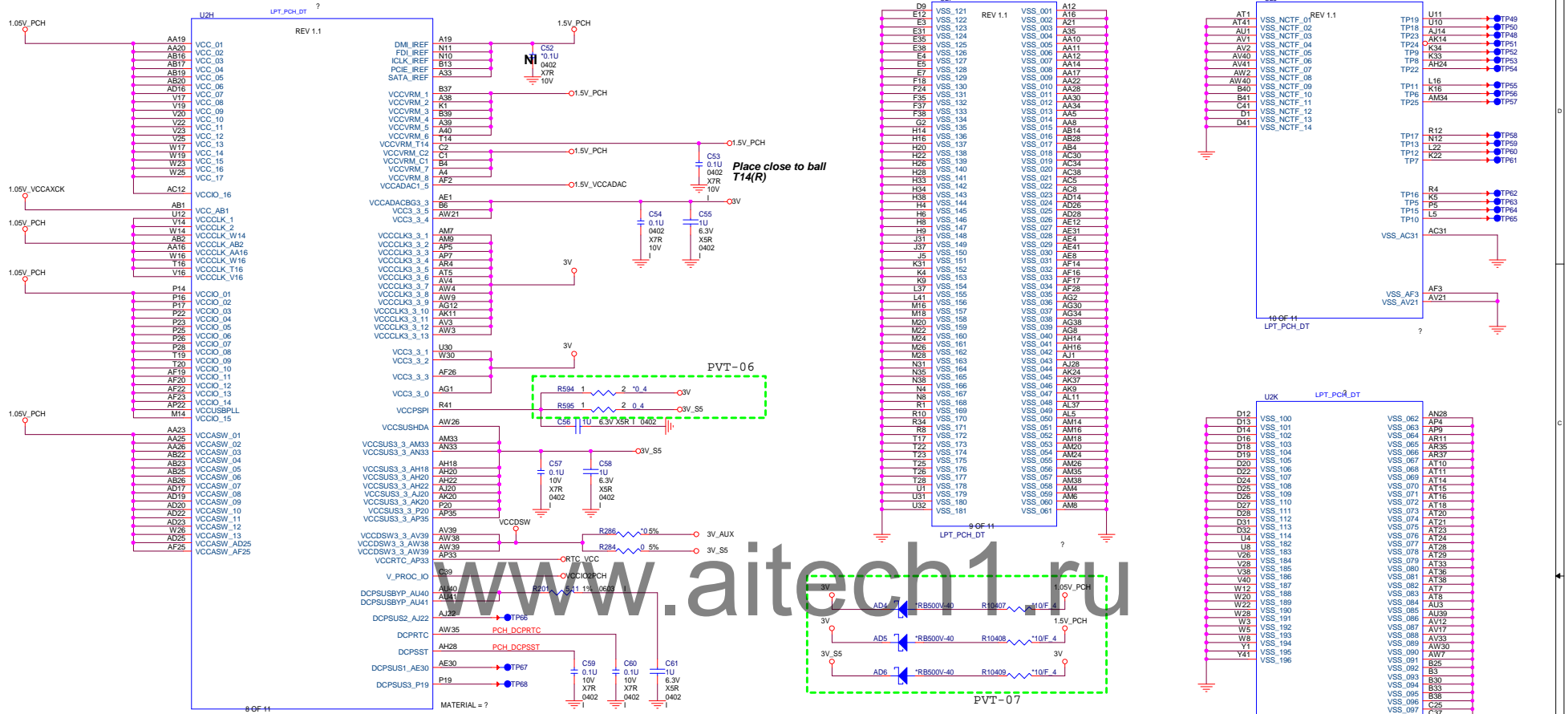


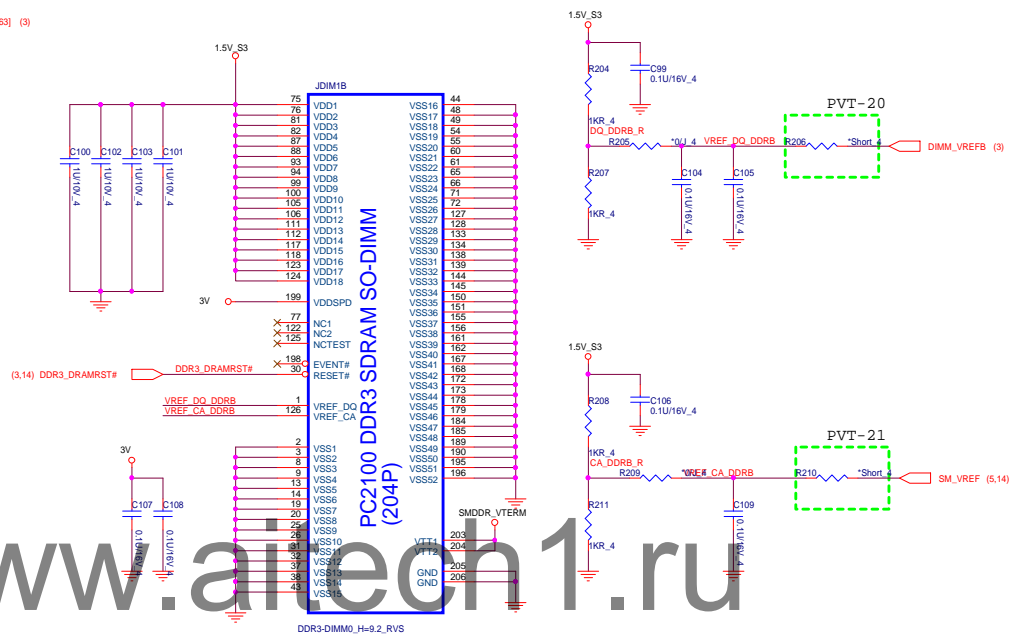
Strap Pin Table

Pin Name	Strap description	Sampled	Configuration	Note												
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	3V 												
GPIO53	Reserved	PWROK	weak internal pull up Should not be pull-down	NC												
GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	3V 												
INTVRMEN	Integrated VRM Enable	ALWAYS	Should be always pull-up	RTC_VCC 												
GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>Bit 1</th><th>Bit 0</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>1</td><td>SPI (default)</td></tr><tr><td>1</td><td>0</td><td>PCI</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table>	Bit 1	Bit 0	Boot Location	1	1	SPI (default)	1	0	PCI	0	0	LPC	3V 
Bit 1	Bit 0	Boot Location														
1	1	SPI (default)														
1	0	PCI														
0	0	LPC														
SATA1GP/GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		WEAK INTERNAL PULLUPS ON BOTH PIN. DEFAULT SPI BOOT DEVICE.												
SATA2GP/GPIO36	Intel Reserved	PWROK	weak internal pull-down This signal should not be pulled high when strap is sampled.	GPIO36 												
SATA3GP/GPIO37	TLS Confidentiality	PWROK	0 = Default, Intel ME Crypto TLS with NO confidentiality 1 = Intel ME Crypto TLS with confidentiality	GPIO37 												
HDA_SDO	Flash Descriptor Security Override /ME Debug Mode	PWROK	weak Internal pull-down 0 = Default 1 = Override	3V_SS 												
HDA_DOCK_EN#/GPIO33	Intel Reserved	PWROK	weak internal pull-down This signal should not be pulled high when strap is sampled.	UNUSE, NC												
GPIO62/ SUSCLK	PLL On-die PWR Voltage regulator Enable	RSMRST#	0 = Disable 1 = Enable (Default)	NC, Use Default												
DDPB_CTRLDATA	Port B detection	PWROK	0 = Default, not detected 1 = Detected	3V 												
DDPC_CTRLDATA	Port C detection	PWROK	0 = Default, not detected 1 = Detected	3V 												
DDPD_CTRLDATA	Port D detection	PWROK	0 = Default, not detected 1 = Detected	3V 												
DSWVRMEN	Deep Sx well on die regulator enable	ALWAYS	0 = Disable 1 = Enable	RTC_VCC 												
GPIO8	Intel Reserved	RSMRST#	This signal must be pulled low when strap is sampled.													

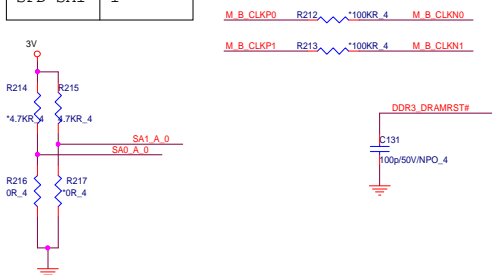




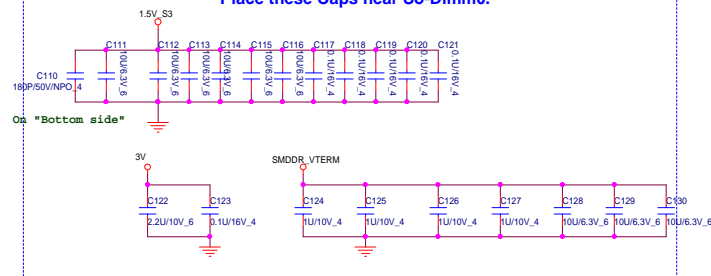


[illegible]

SPD SA0	0
SPD SA1	1



Place these Caps near So-Dimm0.



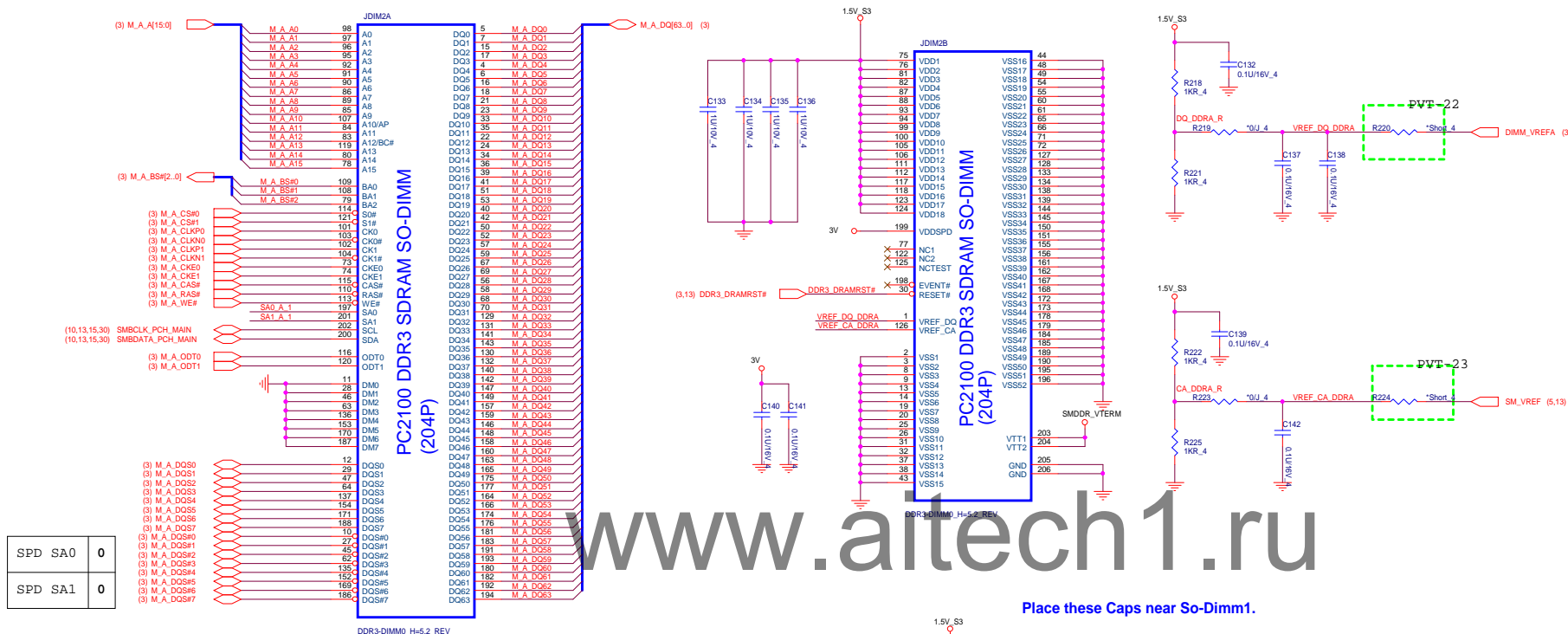
CONFIDENTIAL



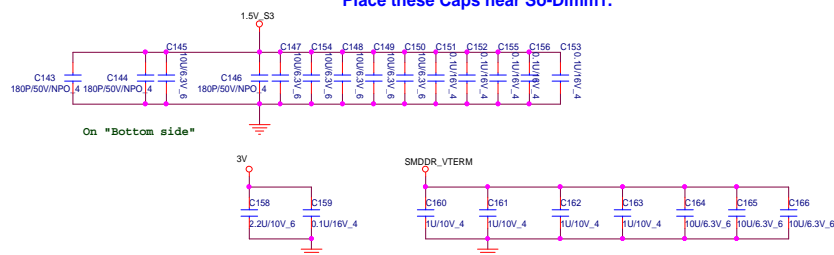
Quanta Computer Inc.
PROJECT : HP ELM

Size	Document Number	DDR3 CHB DIMM0	Rev
Date:	Monday, September 30, 2013	Sheet 13 of 44	

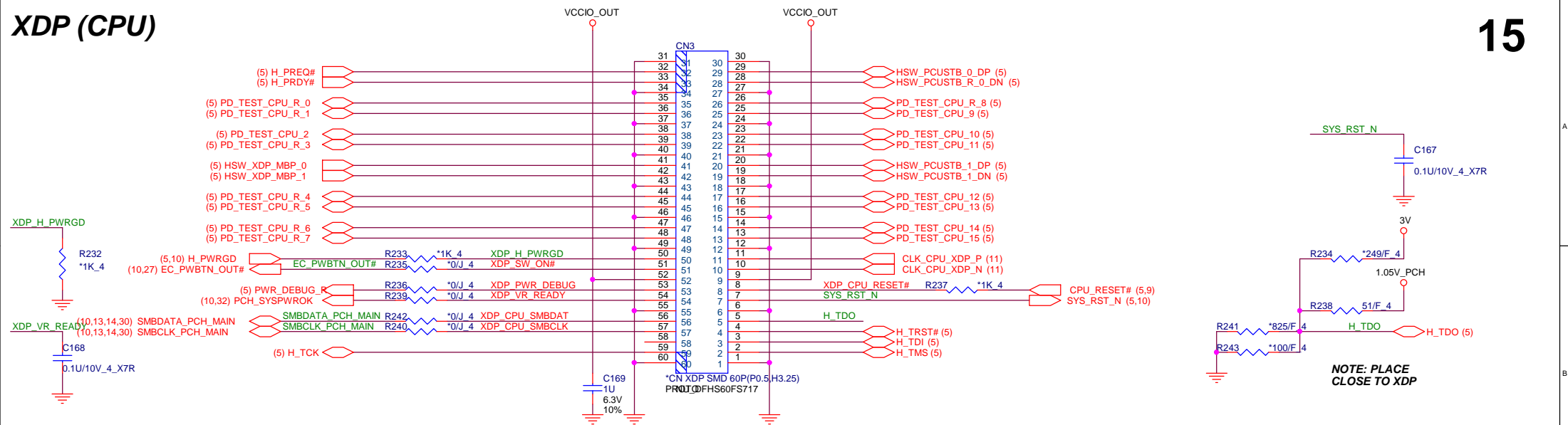
CHANNEL A DIMM 0 H5.2



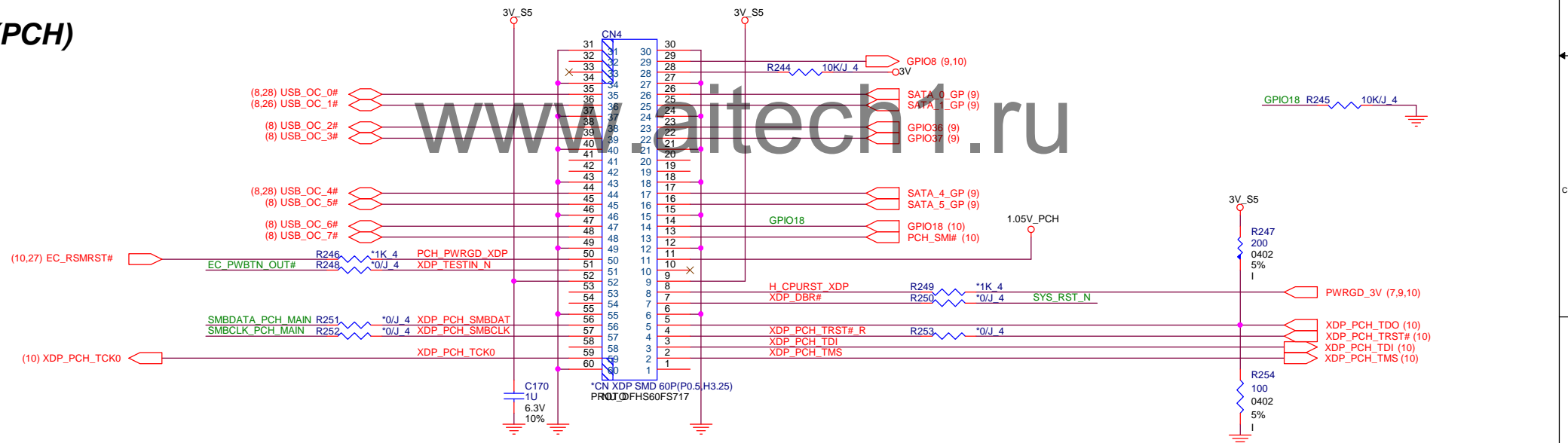
Place these Caps near So-Dimm1.



XDP (CPU)



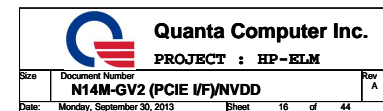
XDP (PCH)

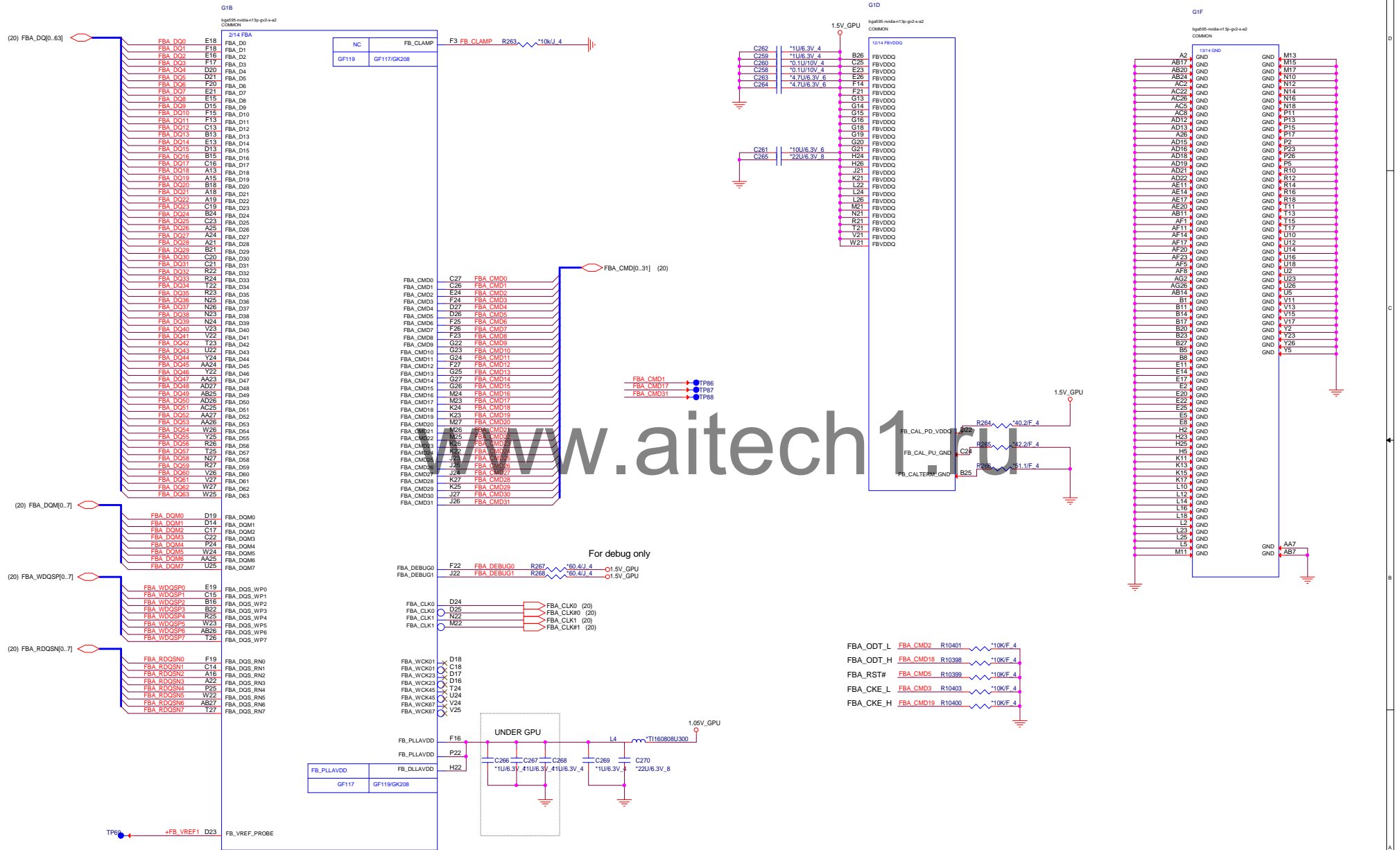


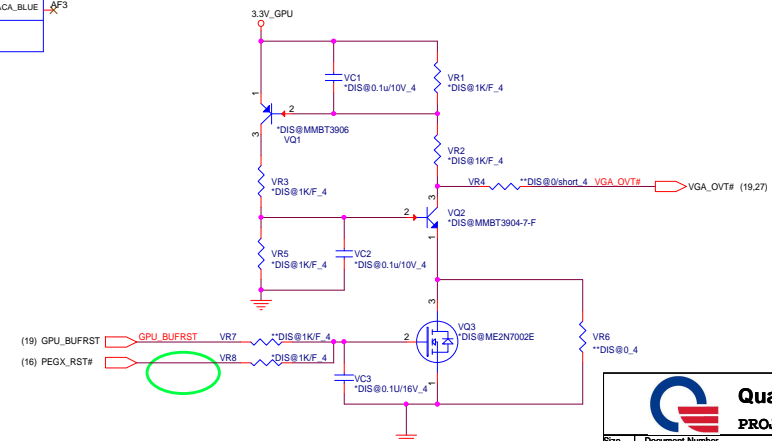
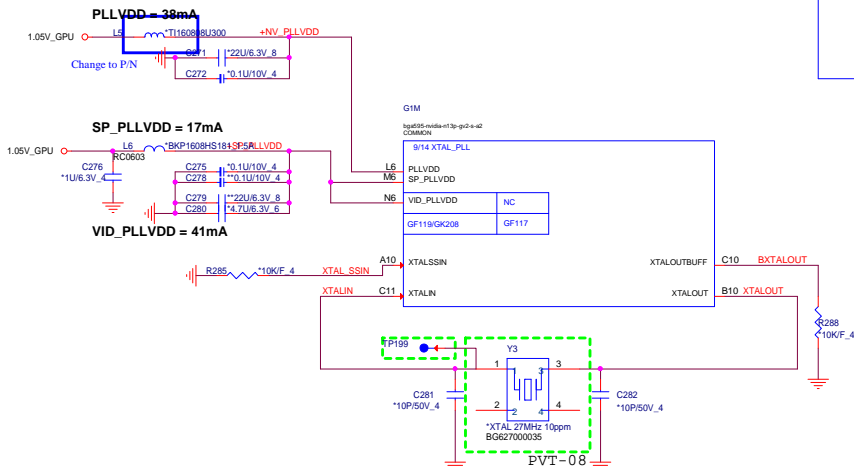
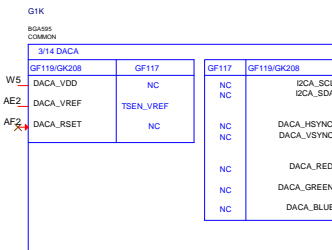
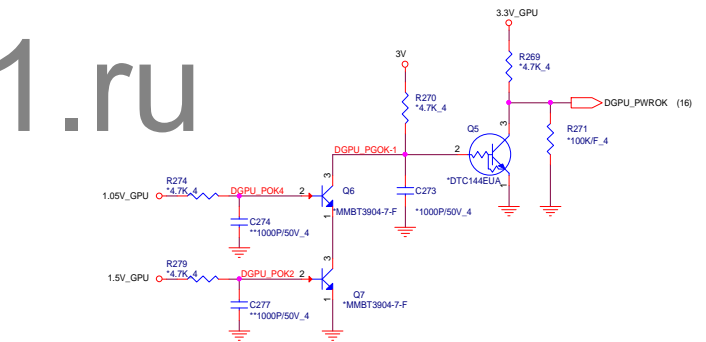
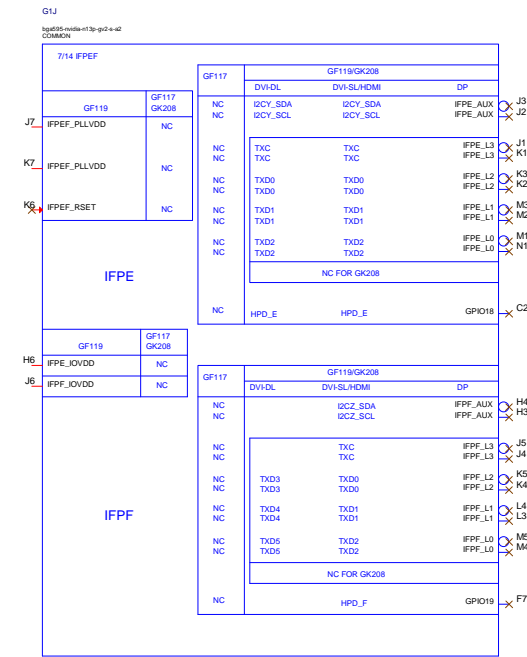
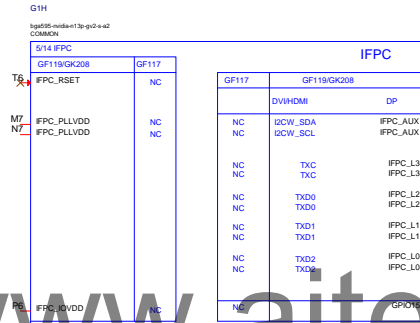
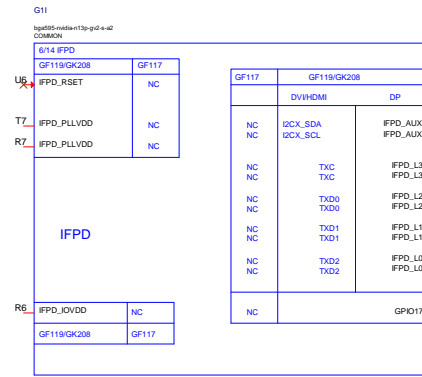
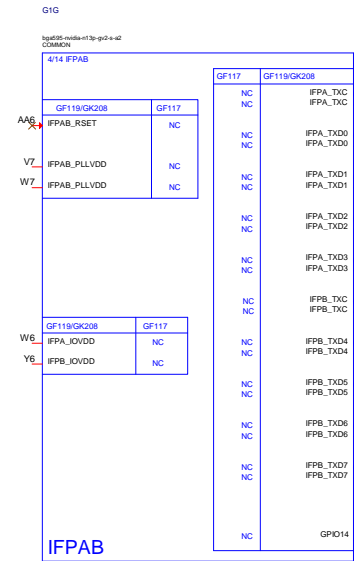
Quanta Computer Inc.

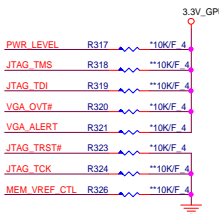
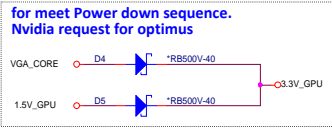
PROJECT : HP-ELM

Size	Document Number	Rev
	XDP DEBUG	A
Date:	Monday, September 30, 2013	Sheet 15 of 44







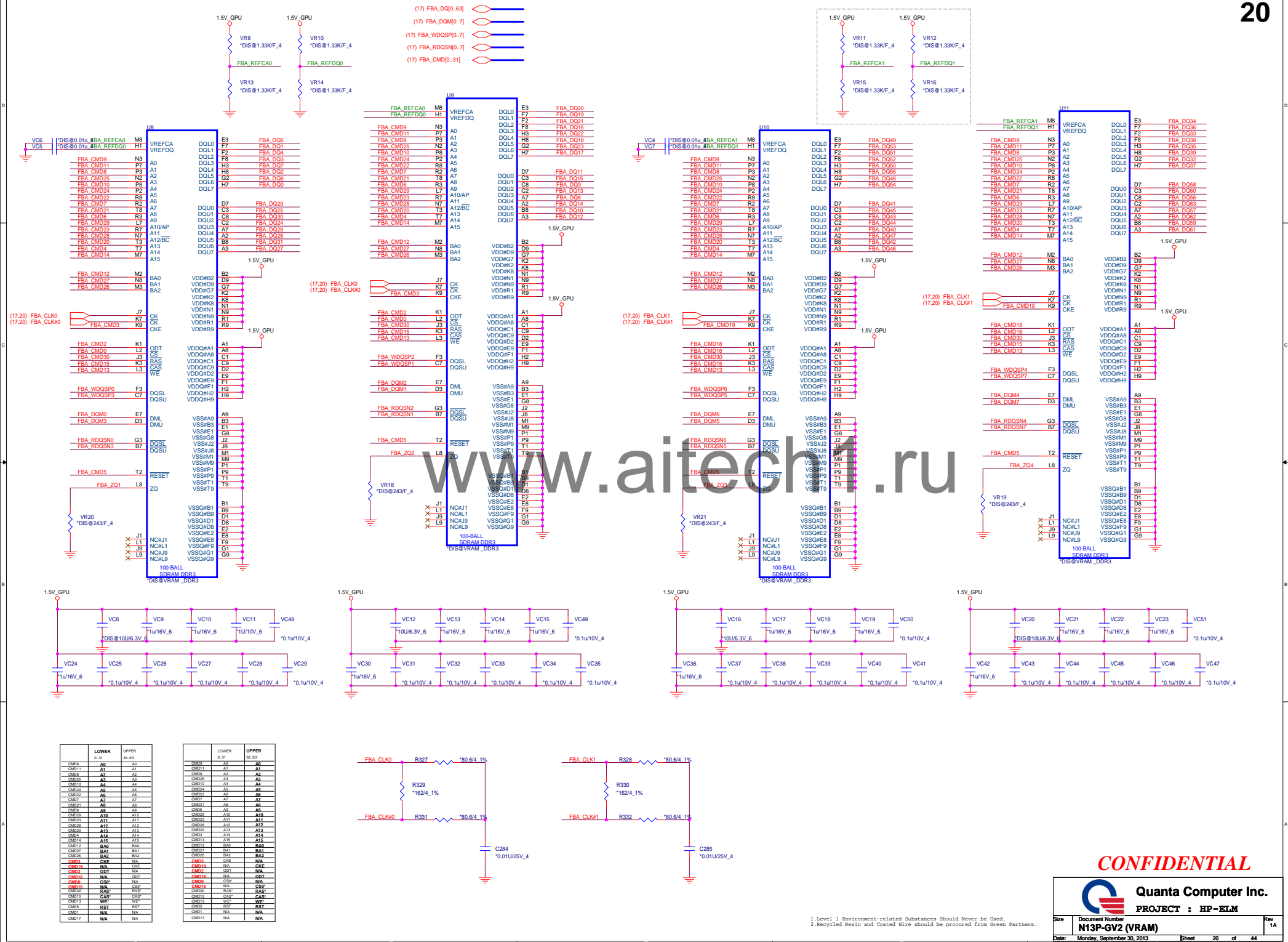
[illegible]Table 121. Resistance Mapping to Hex Values

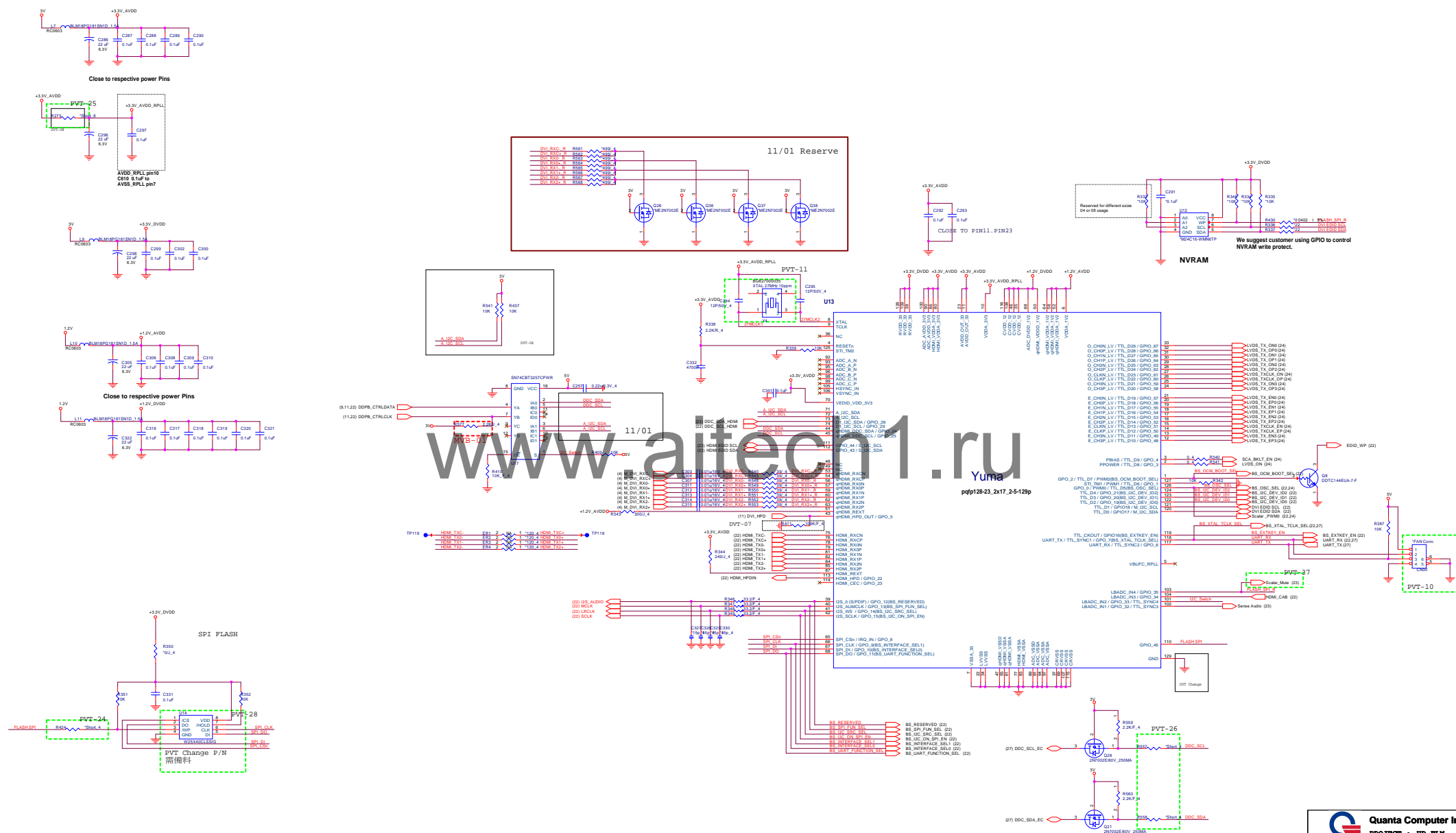
Register Values	Pull up to VDD33	Pull down to GND
-----------------	------------------	------------------

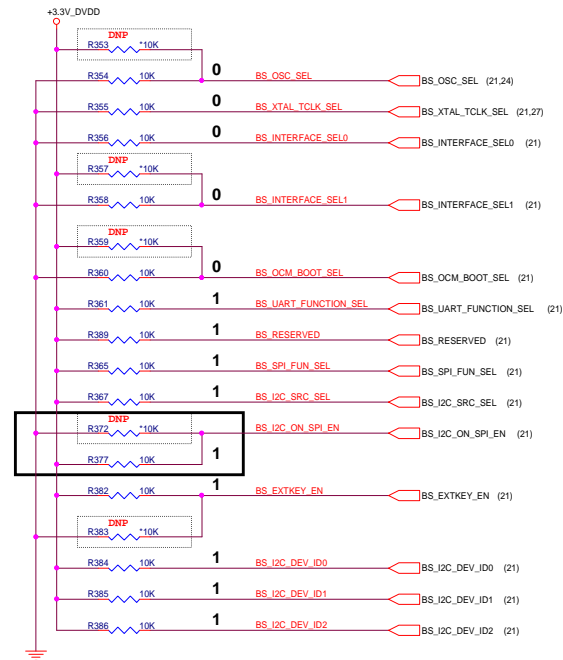
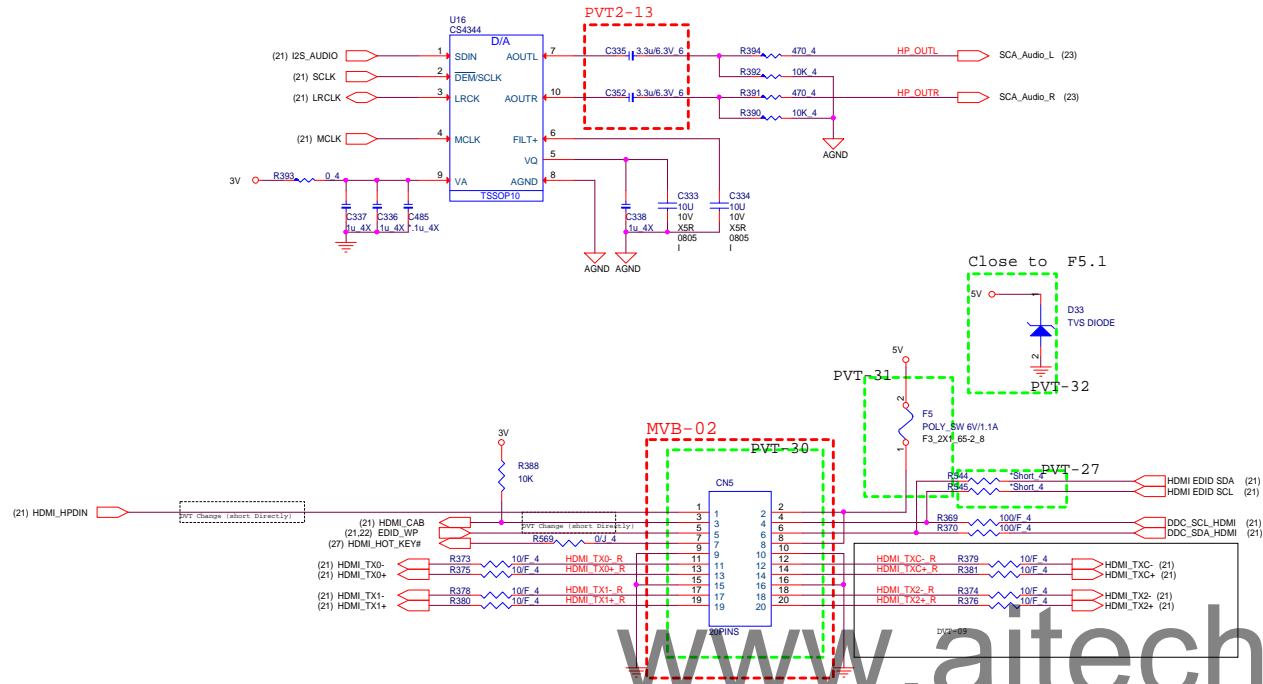
ROM_SI pin is resistance
mapping to Hex

PVT2-17

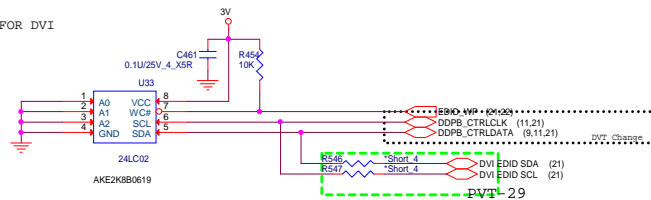






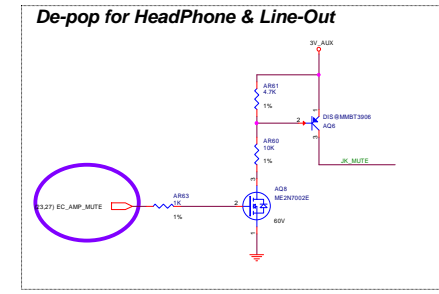
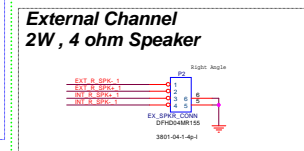
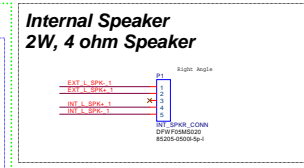
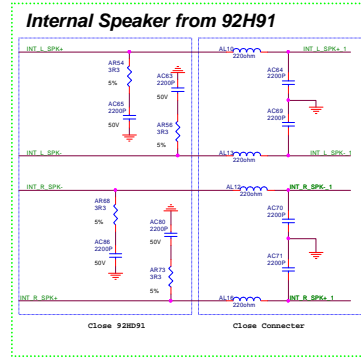
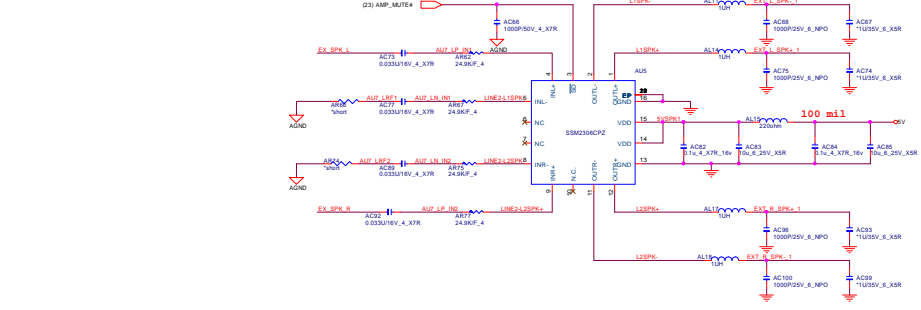
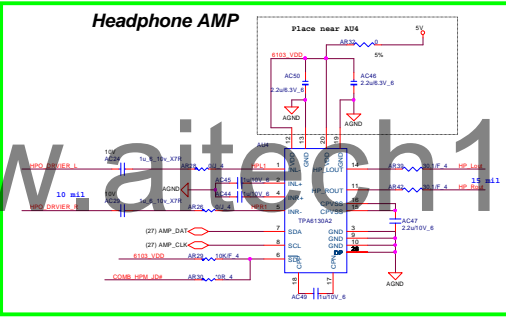
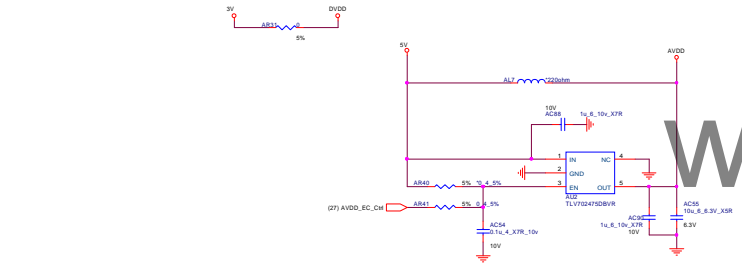
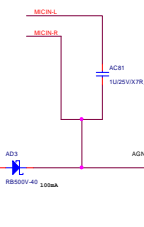
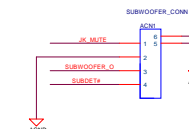
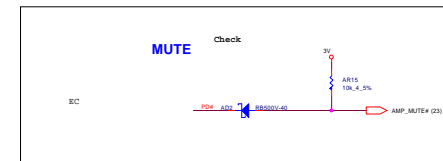
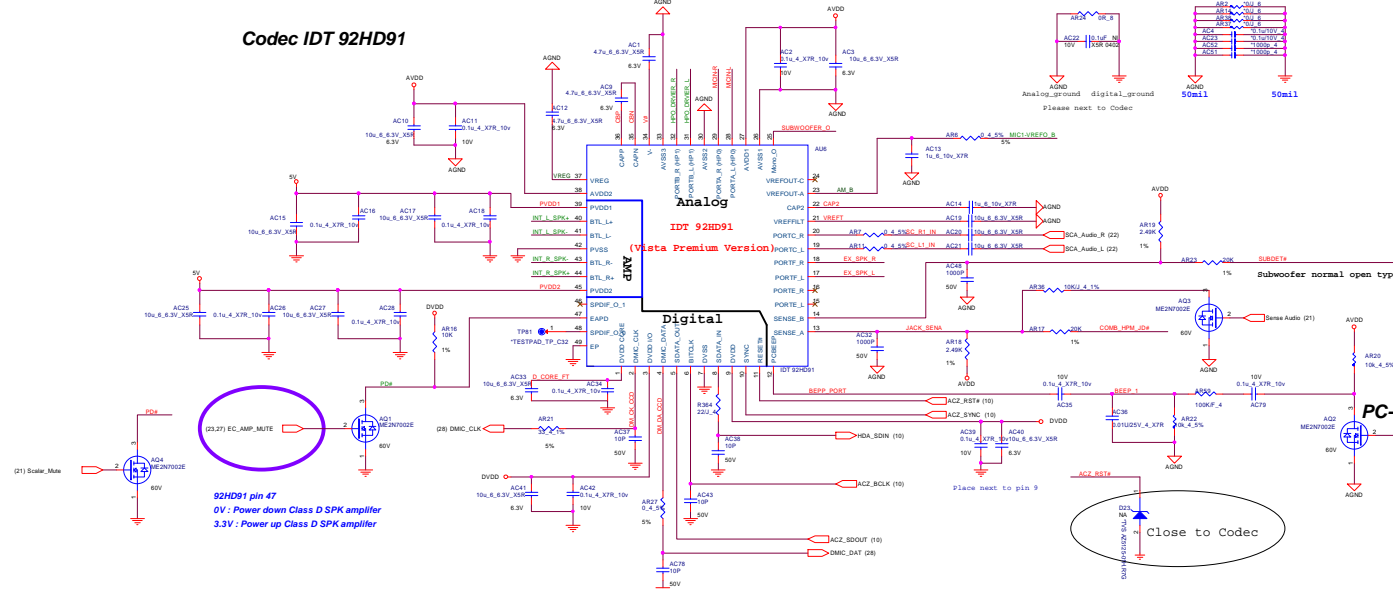


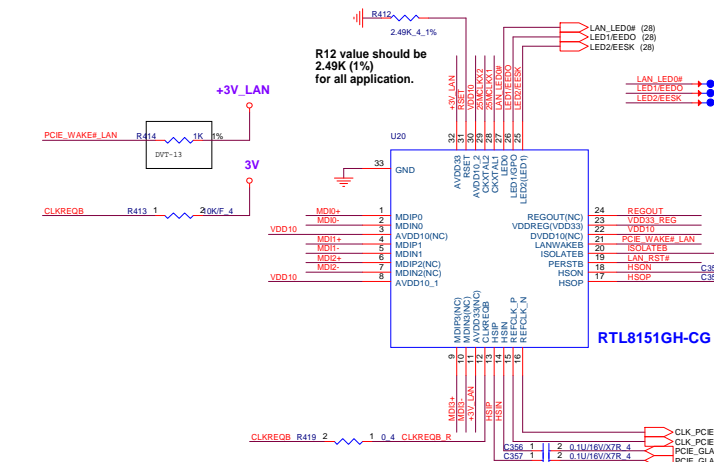
EDID FOR DVI



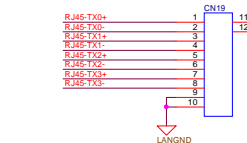
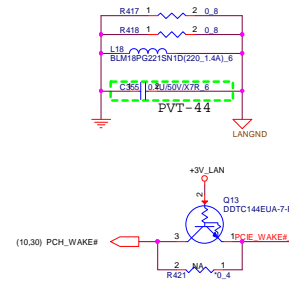
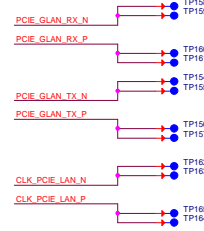
Bootstrap configuration:

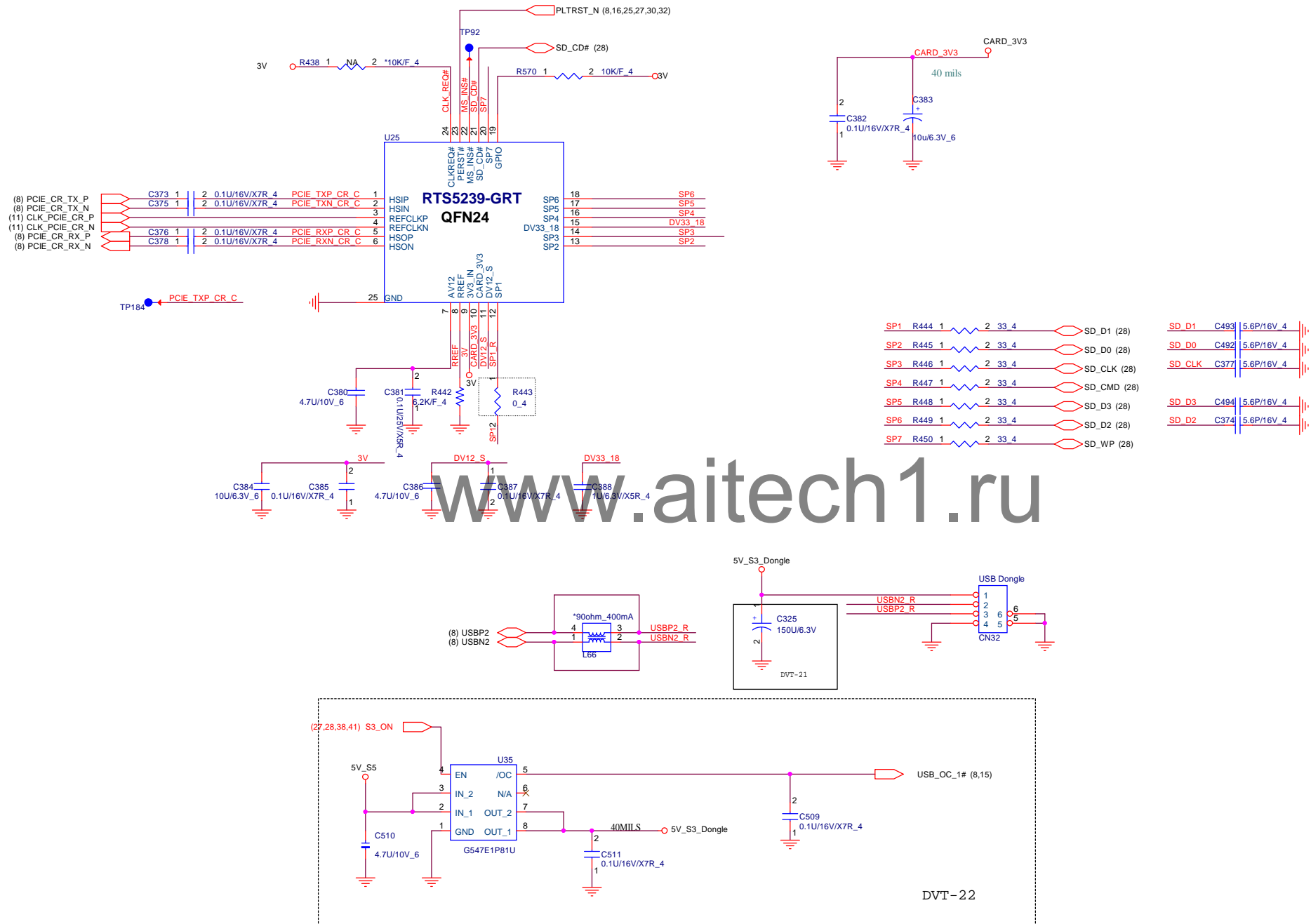
OSC_SEL	MUST BE PROGRAMMED TO 0
XTAL_TCLK_SEL	0 = XTAL & INTERNAL OSC TO DRIVE TCLK
INTERFACE_SEL0	MUST BE PROGRAMMED TO 0
INTERFACE_SEL1	0 = GPIO[27:26] ARE DDC VGA FUNCTION 1 = GPIO[27:26] ARE JTAG FUNCTION (DEBUG PURPOSE)
OCM_BOOT_SEL	0 = OCM BOOT FROM INTERNAL ROM 1 = OCM BOOT FROM EXTERNAL ROM
UART_FUN_SEL	1 = UART IS ENABLED
RESERVED	MUST BE PROGRAMMED TO 1
SPI_FUN_SEL	1 = SPI INTERFACE IS ENABLED
I2C_SRC_SEL	1 = I2C PINS ARE USED FOR I2C MASTER
I2C_ON_SPI_EN	0 = I2C PINS ARE AT GPIO43/44 1 = I2C PINS ARE AT SPI INTERFACE GPIO43/44 function could be used.
EXTKEY_EN	0 = NORMAL MODE OF OPERATION 1 = OTP KEY MANAGER TO USE EXTERNAL STORAGE FOR ACCESS TO COPY PROTECTION KEYS
I2C_DEV_ID2	I2C ADDRESS IN SLAVE MODE 111 = 0XC0, 0XC1
I2C_DEV_ID1	110 = 0XC2, 0XC3
I2C_DEV_ID0	101 = 0XC4, 0XC5 100 = 0XC6, 0XC7 011 = 0XE0, 0XE1 010 = 0XE2, 0XE3 001 = 0XE4, 0XE5 000 = 0XE6, 0XE7

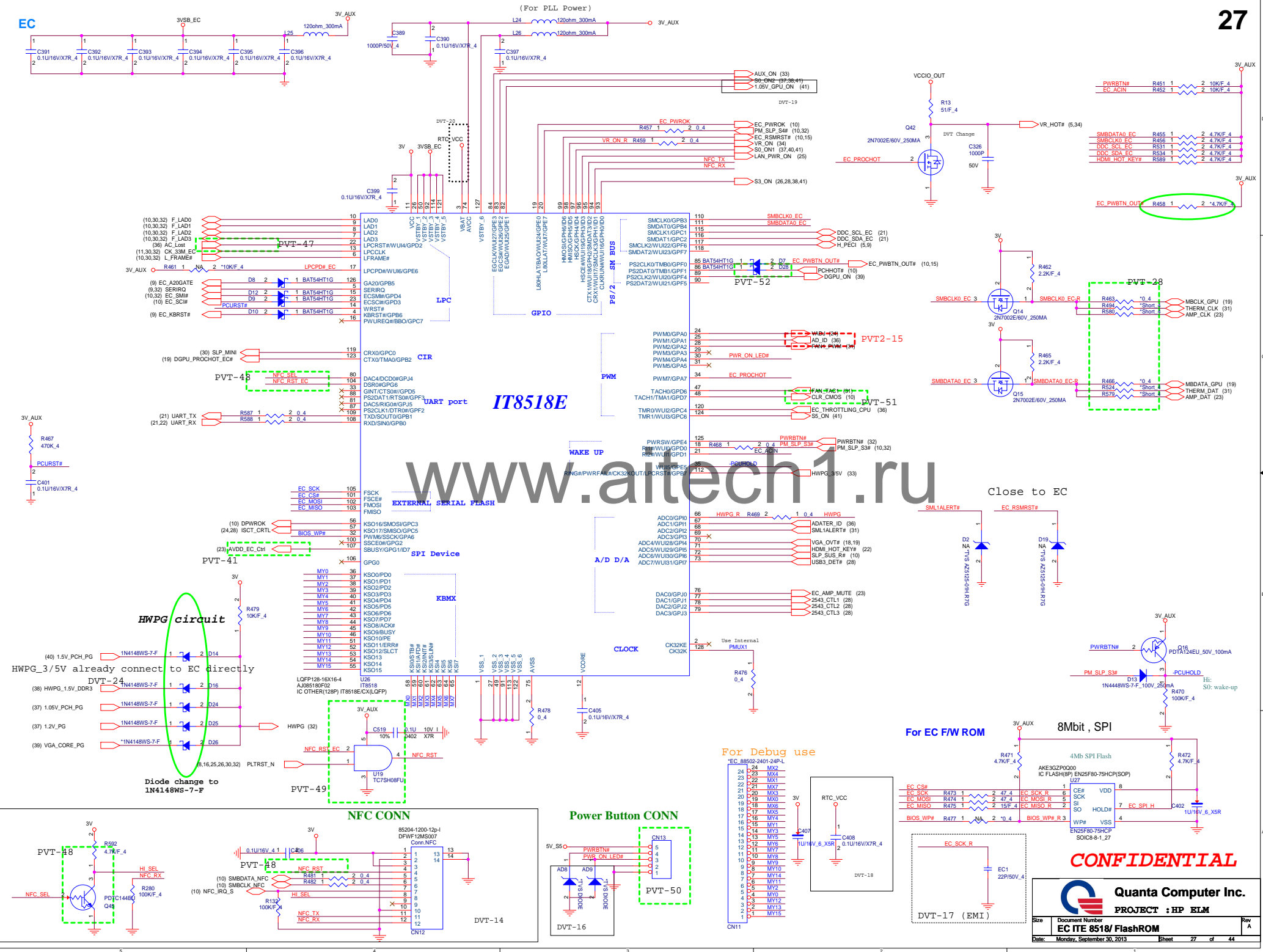




(RTL8151GH-CG) 10/100/1000
AL008151B00

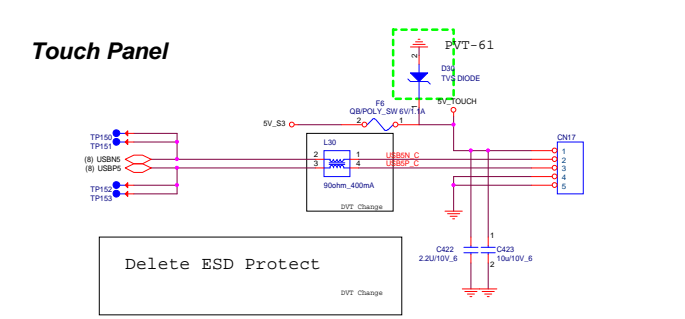
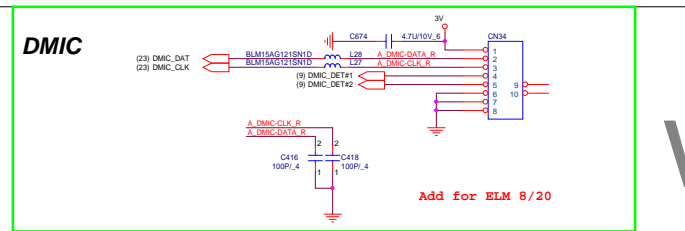
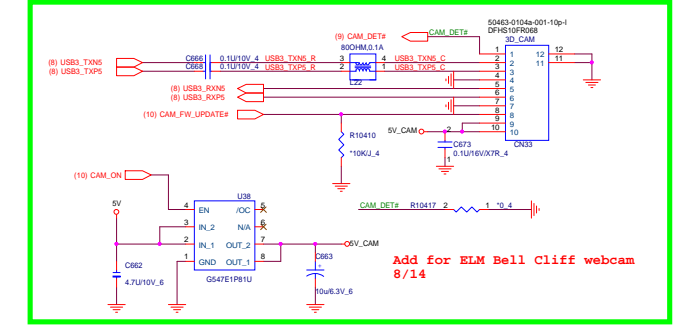
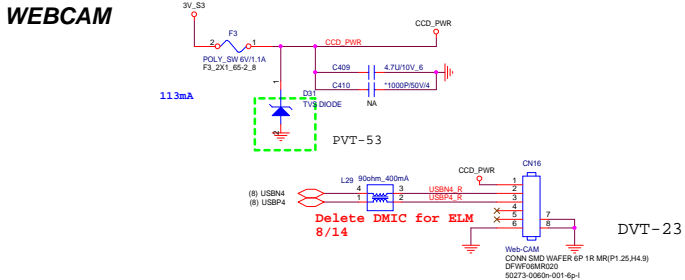




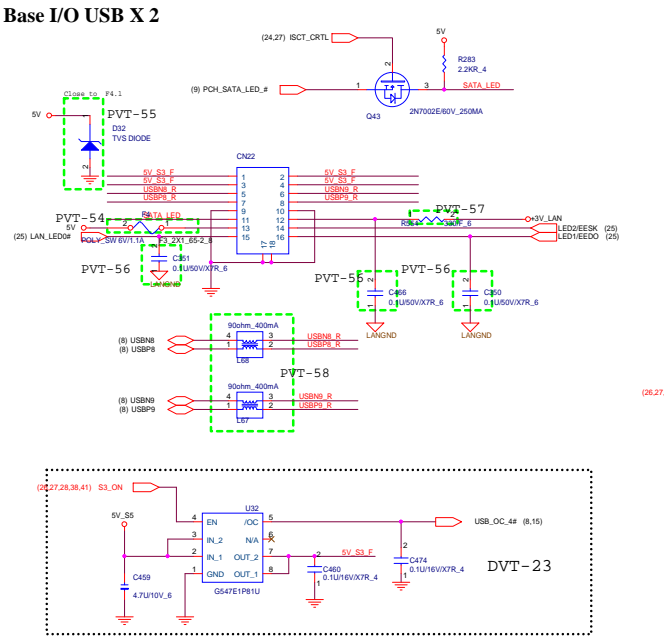


CONFIDENTIAL

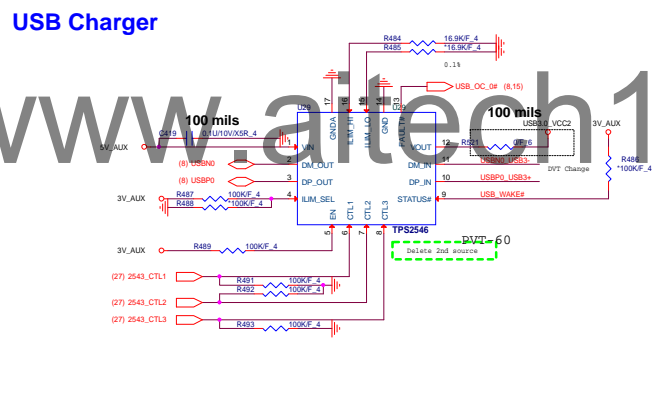
WEBCAM



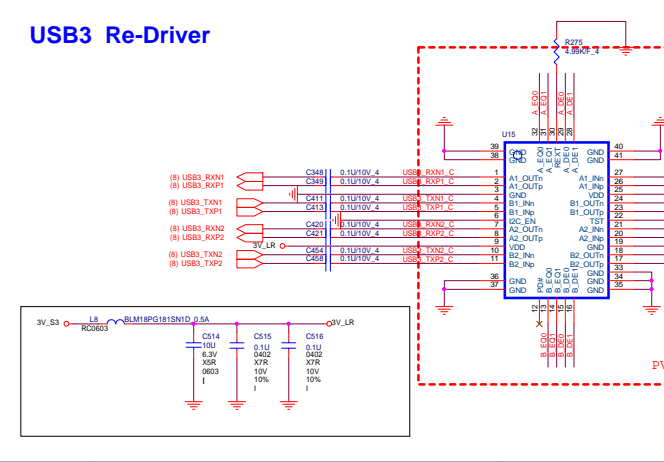
Base I/O USB X 2



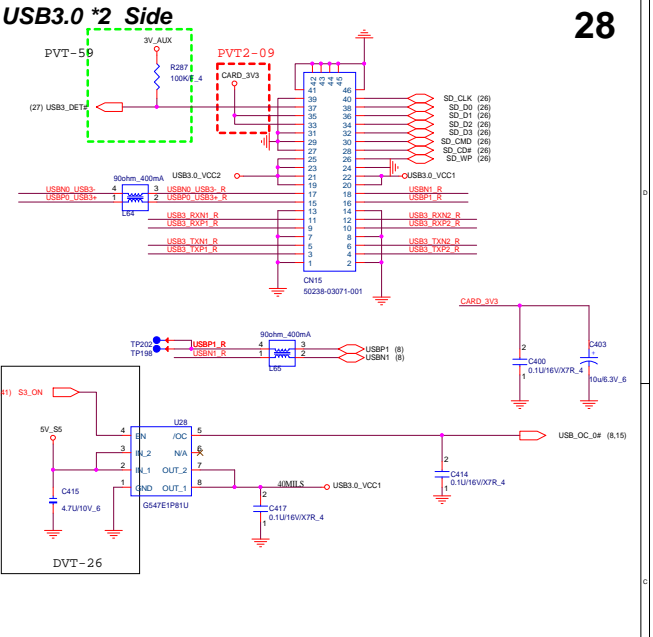
USB Charger



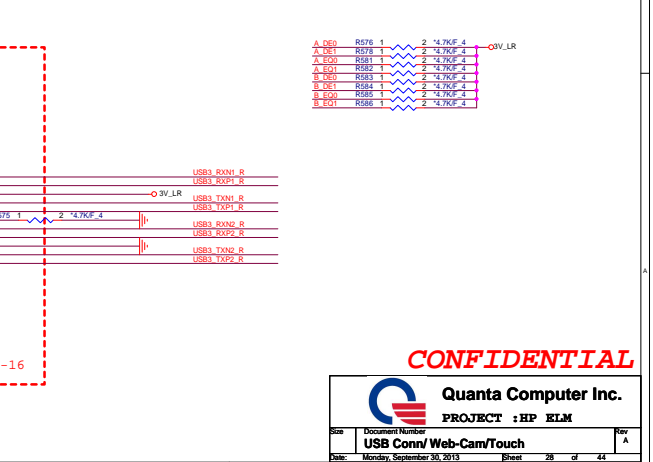
USB3 Re-Driver



USB3.0 *2 Side




POWER STATE	TPS2546 CHARGING MODE	CTRL1	CTRL2	CTRL3	ILIM
S0	CDP LOAD DETECTION WITH ILIM_LO +60mA THRESHOLDS OR IF A BC1.2 PRIMARY DETECTION OCCURS	1	1	1	1
S3	AUTO MODE, LOAD DETECTION WITH POWER WAKE THRESHOLDS	0	1	1	1
S4/S5	AUTO MODE, KEYBOARD/ MOUSE WAKE-UP, LOAD DETECTION WITH ILIM_LO +60mA THRESHOLDS	0	0	1	1



Delete EDP to LVDS IC for ELM
8/14

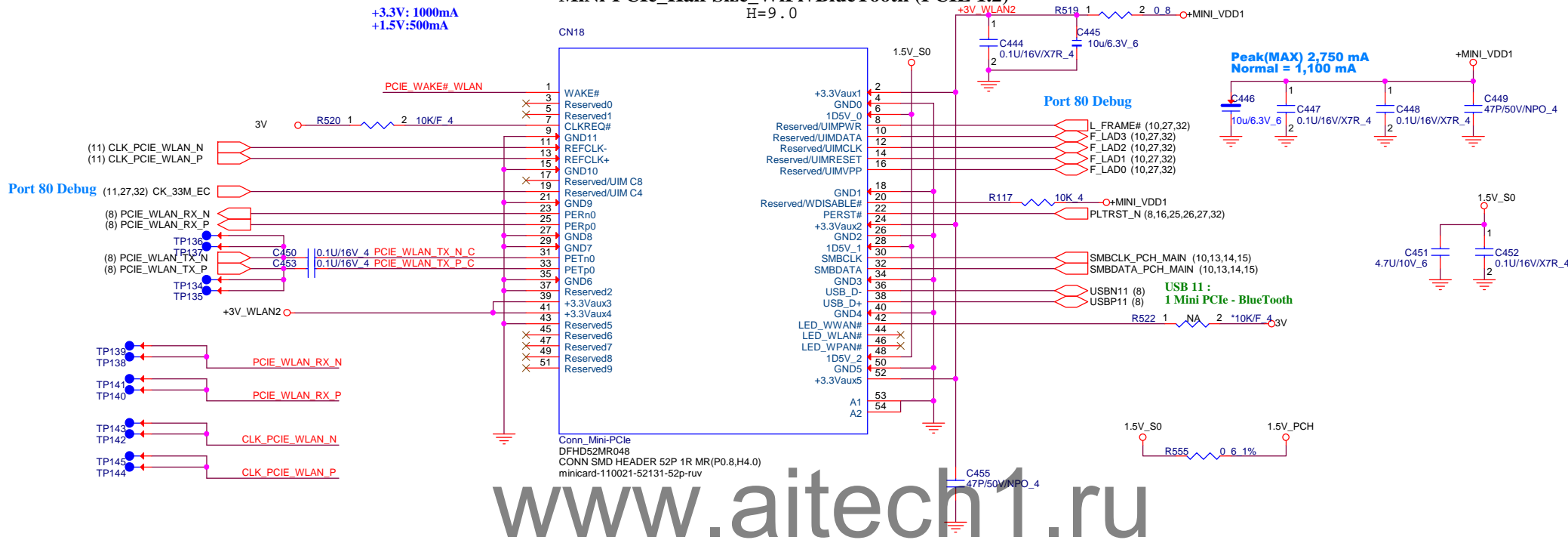
www.aitech1.ru

CONFIDENTIAL

		Quanta Computer Inc.	
PROJECT : HP ELM		Rev 3E	
Size	Document Number	Date	Monday, September 30, 2013
	DP to LVDS	Sheet	29 of 44

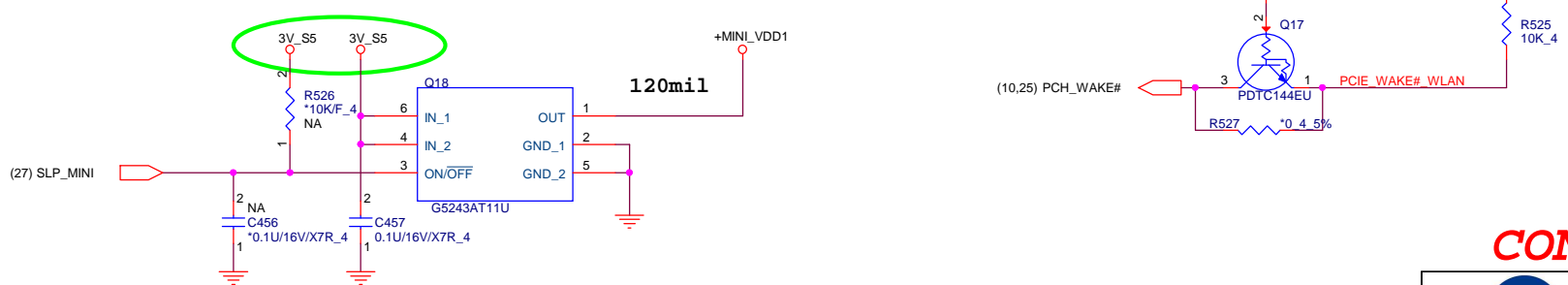
MiNi-PCIe_Half Size_WiFi+BlueTooth (PCIE 1.2)

H=9.0



MiNi PCIe_power(S5)

WLAN_ON Load SW



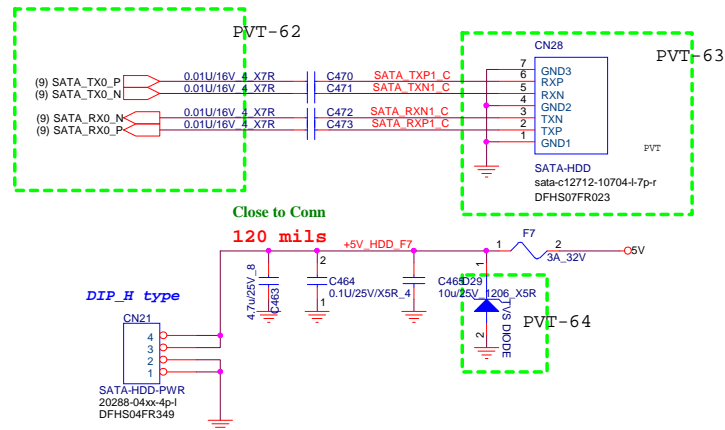
CONFIDENTIAL



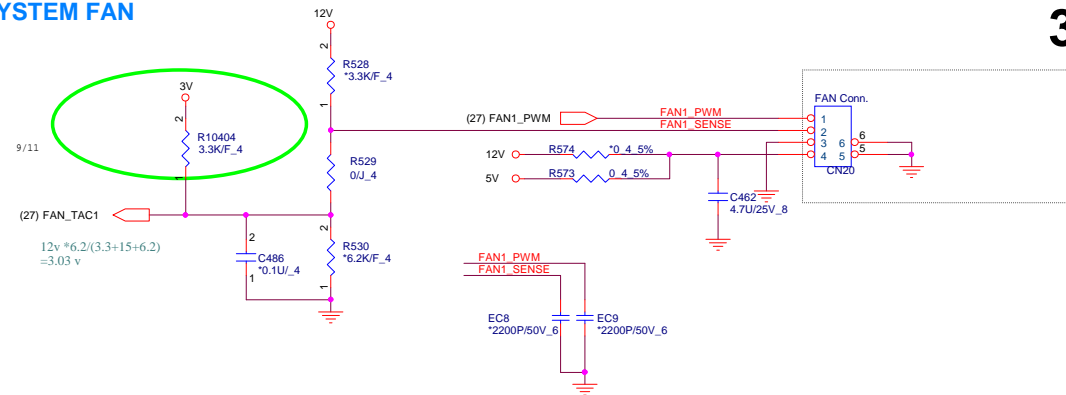
Quanta Computer Inc.
PROJECT : HP ELM

Size	Document Number	Rev
	Mini PCIe WLAN	A
Date:	Monday, September 30, 2013	Sheet 30 of 44

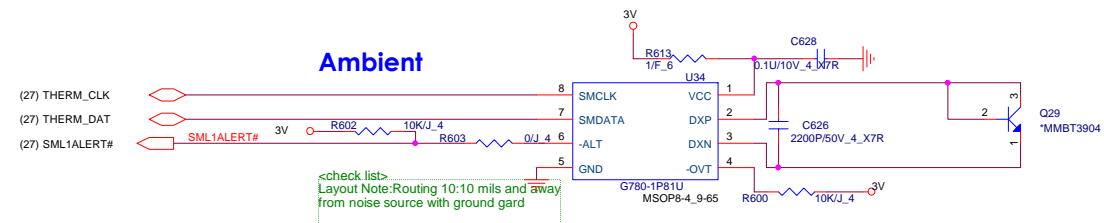
HDD SATA Conn.



SYSTEM FAN

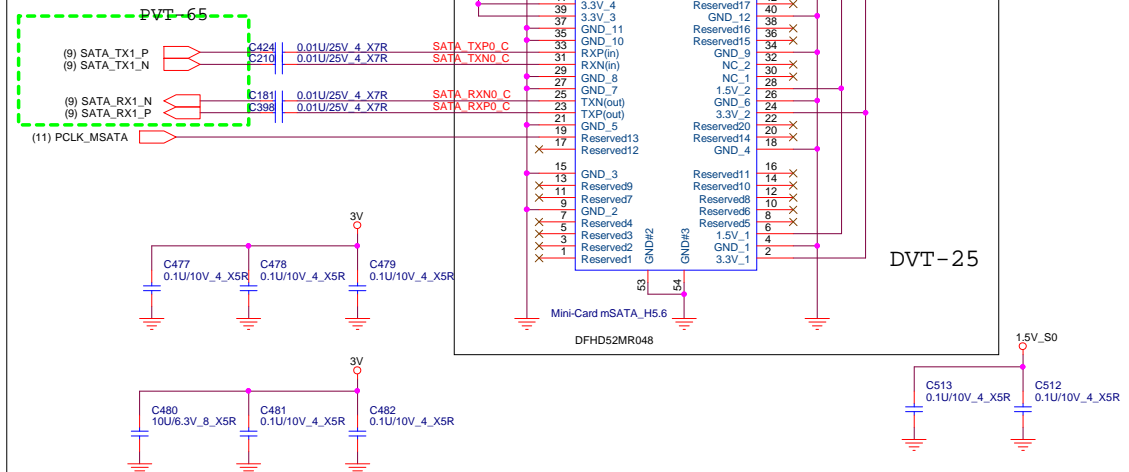
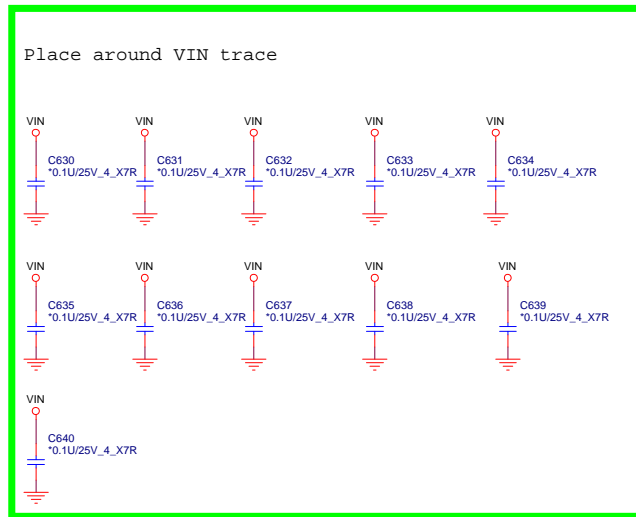


THERMAL SENSOR



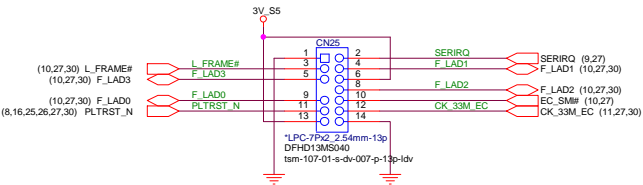
www.aitech1.ru

Mini Card-mSATA

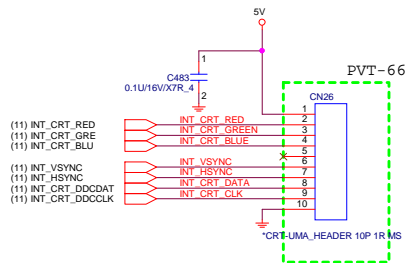


LEDs/LPC HEADER

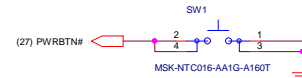
LPC HEADER



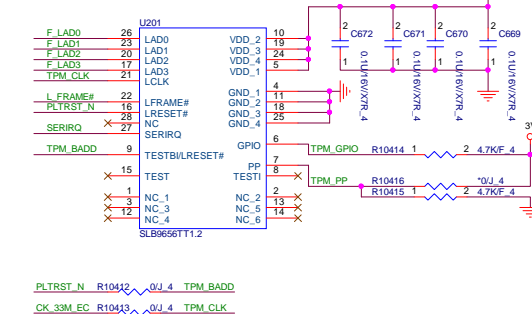
CRT for UMA Debug



SW1 For Debug.MP will remove it.

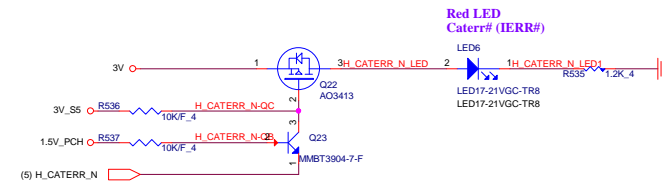
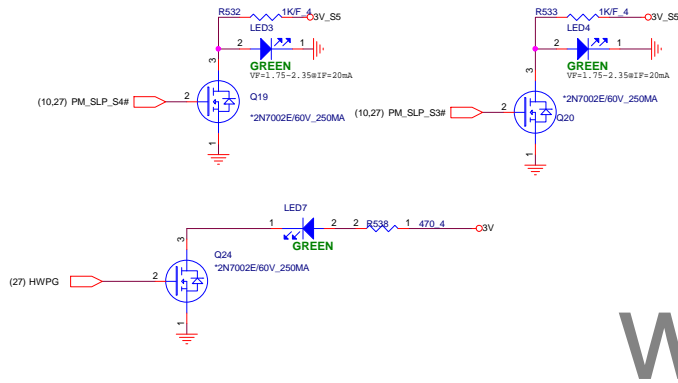


TPM reserved for ELM 1C14 requirement



32

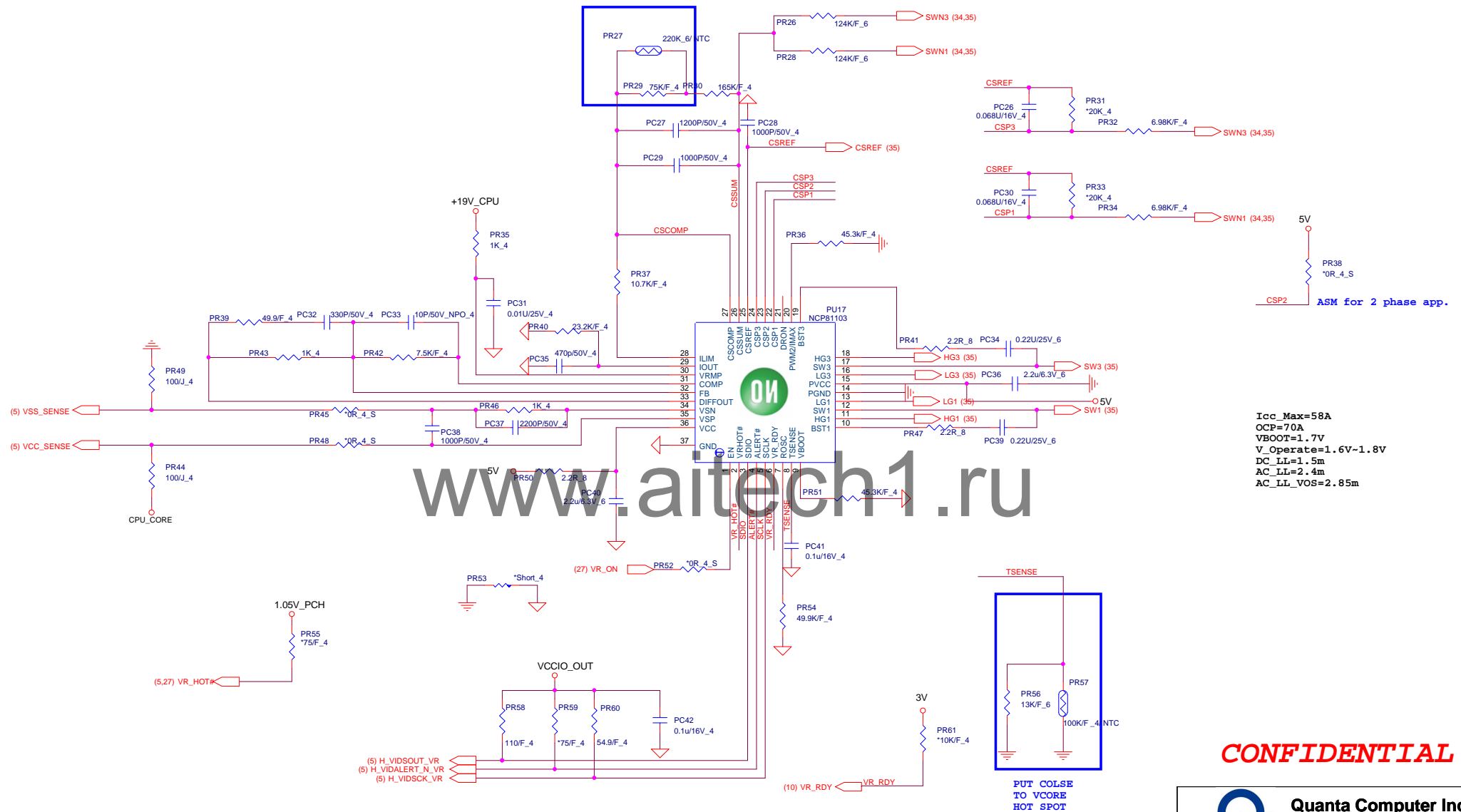
PCA debug LED requirement:



www.aitech1.ru

CONFIDENTIAL





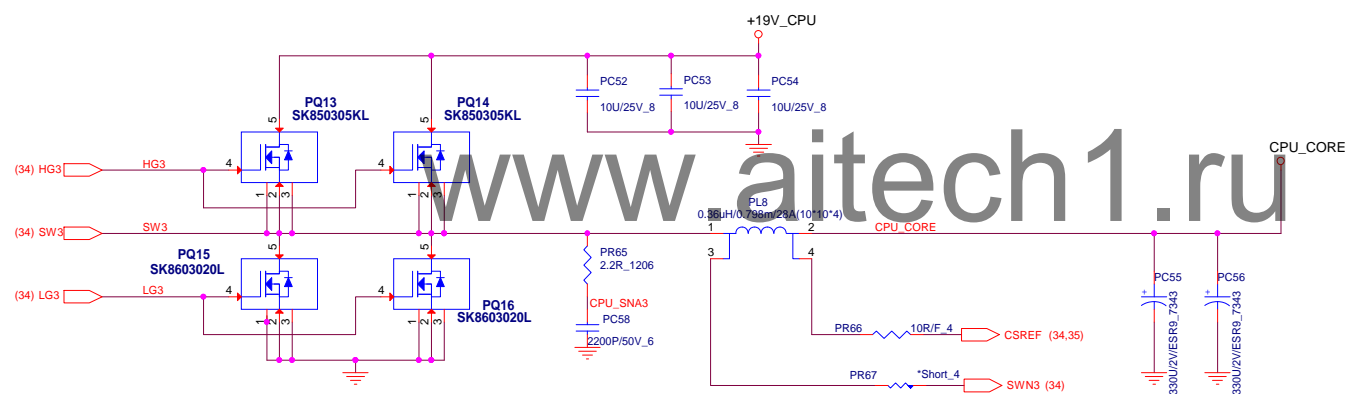
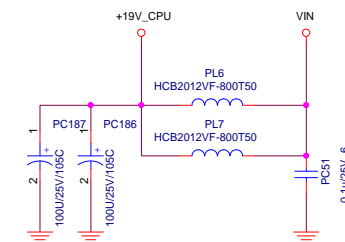
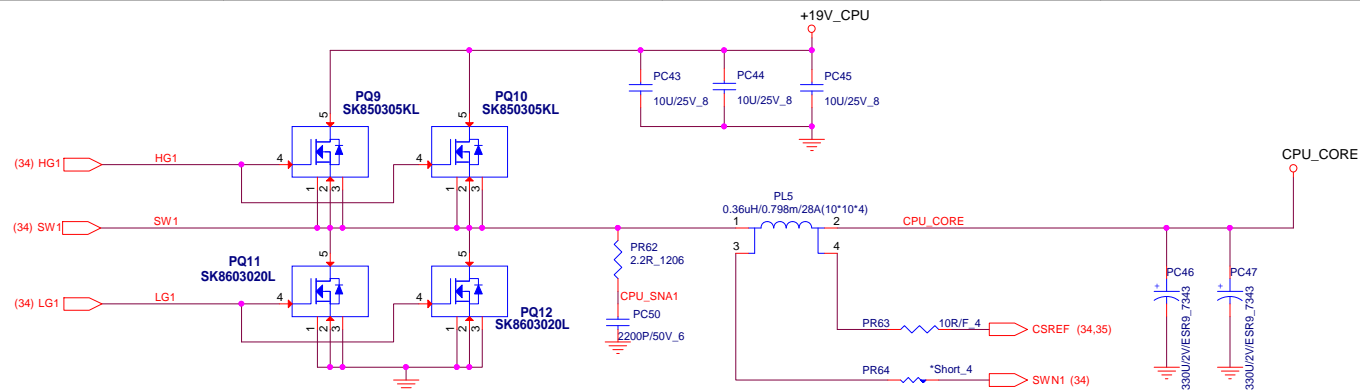
CONFIDENTIAL



Quanta Computer Inc.

PROJECT : HP ELM

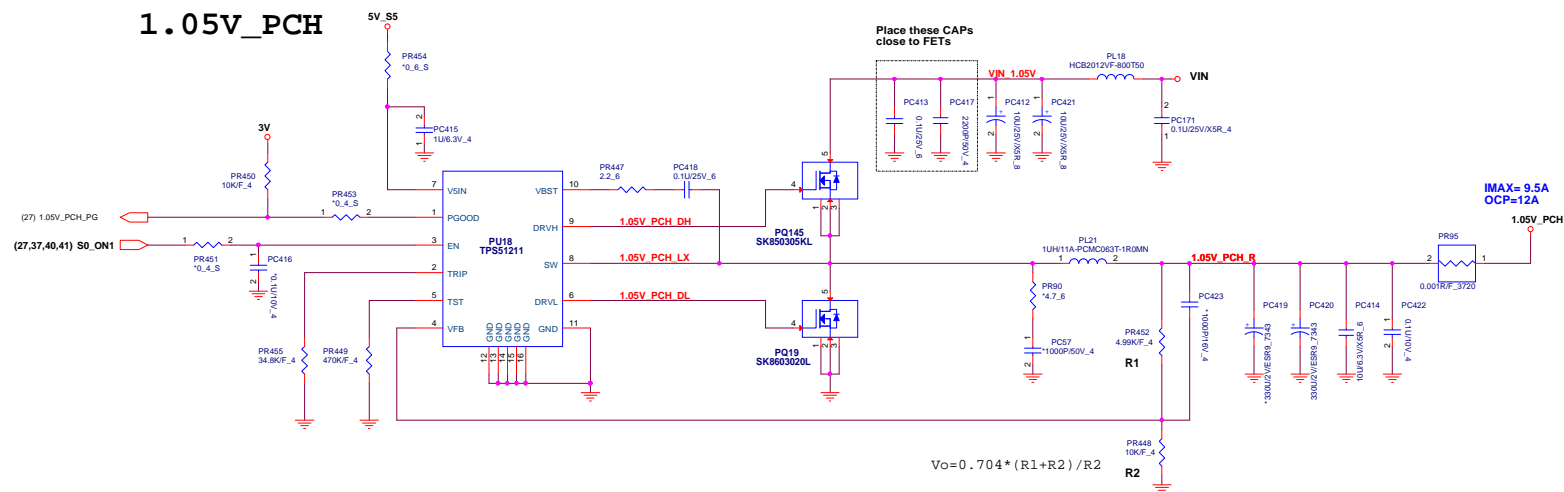
Size	Document Number CPU NCP81103	Rev A
Date:	Monday, September 30, 2013	Sheet 34 of 44



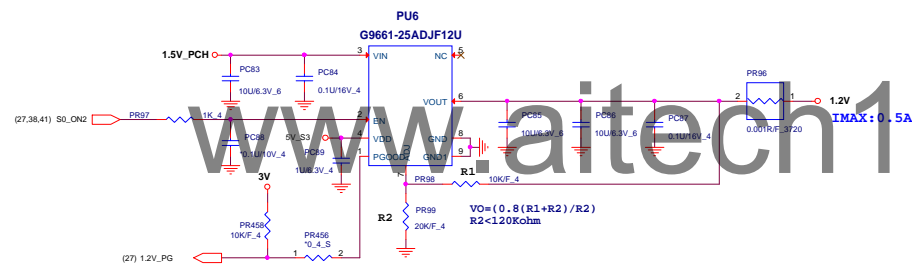


VH_L=1.303V, Triggered current 5.212A/101.6W

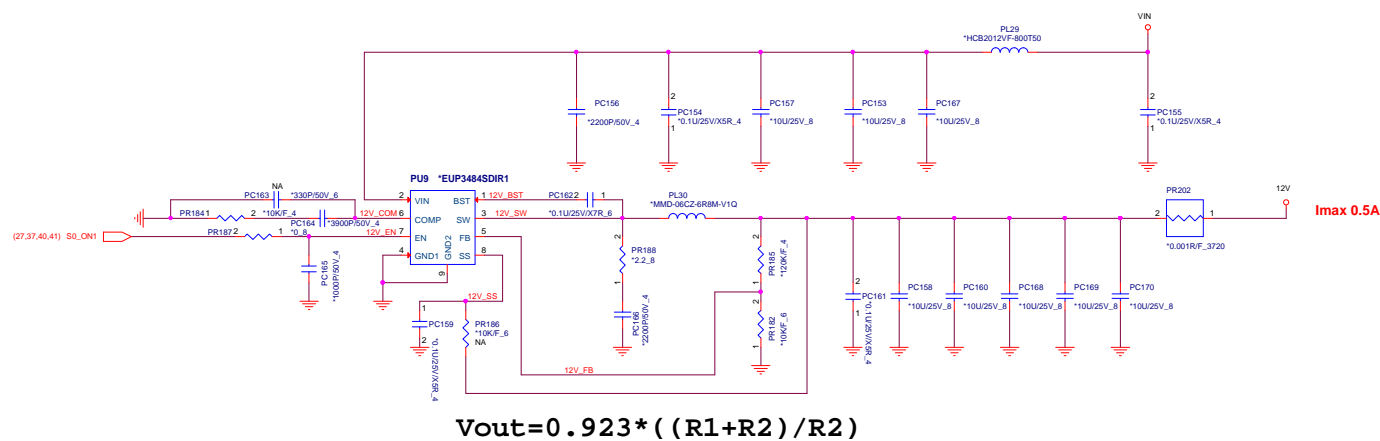
CONFIDENTIAL



1.2V



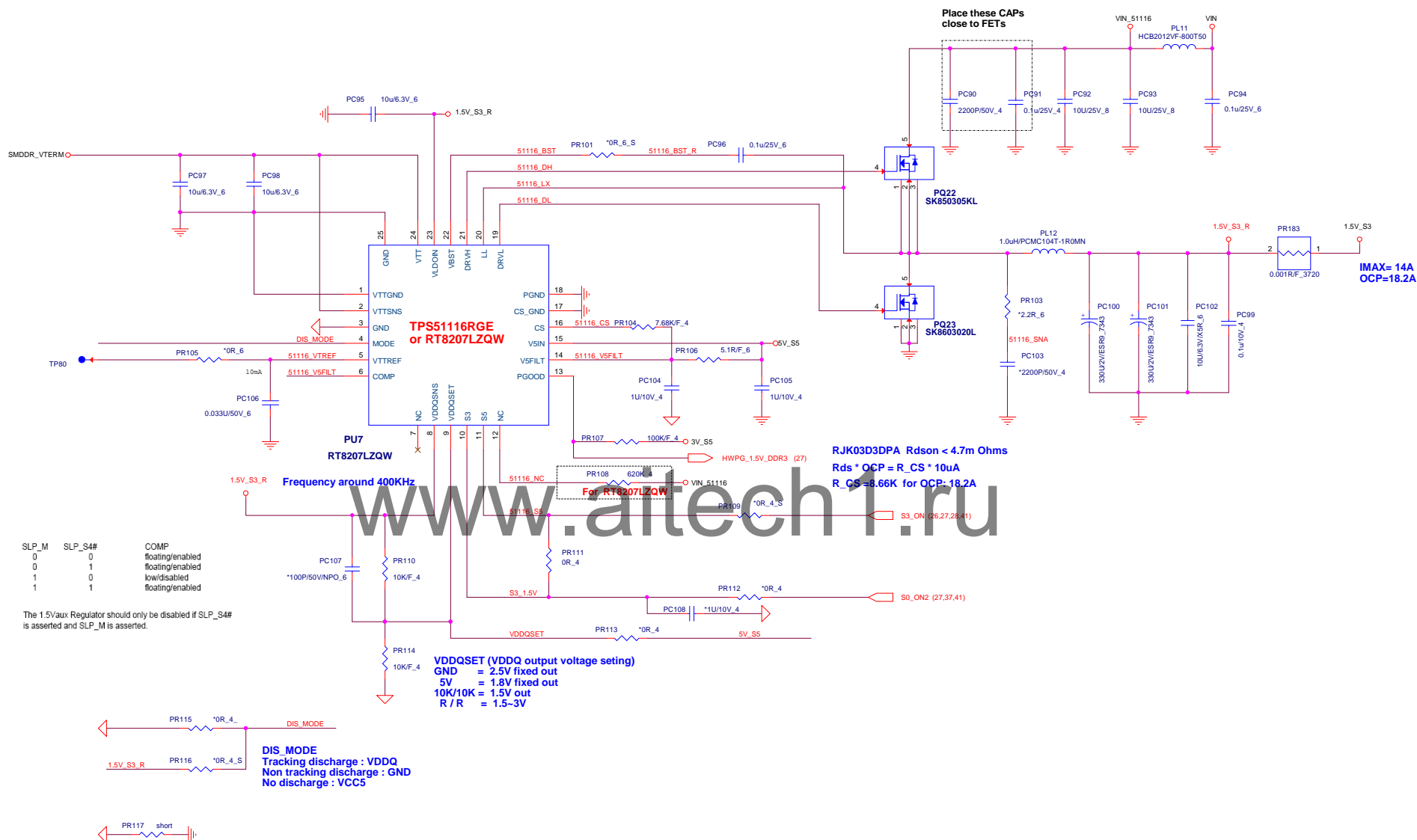
12V



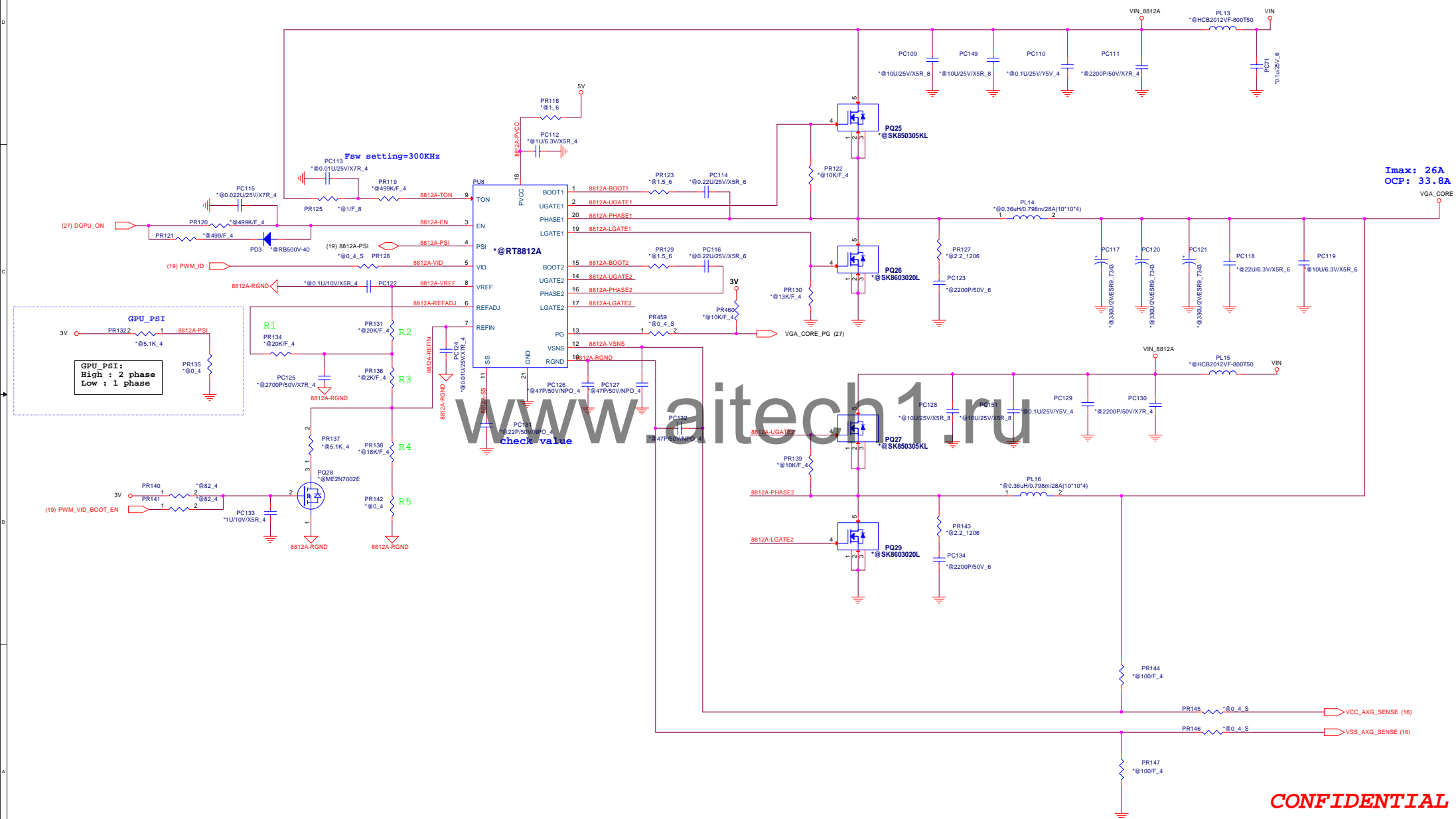
CONFIDENTIAL

Quanta Computer Inc.
PROJECT : HP HAGIA

Doc: Monday, September 30, 2013 Sheet 37 of 44



VGA-CORE

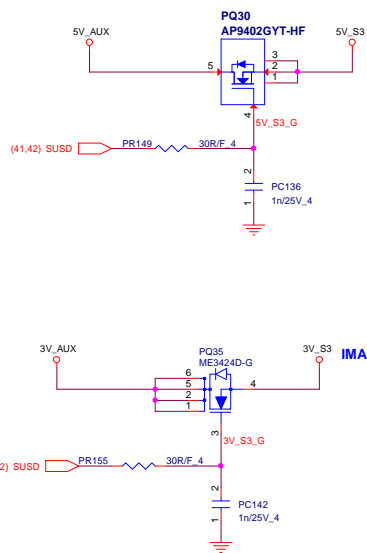
**CONFIDENTIAL**



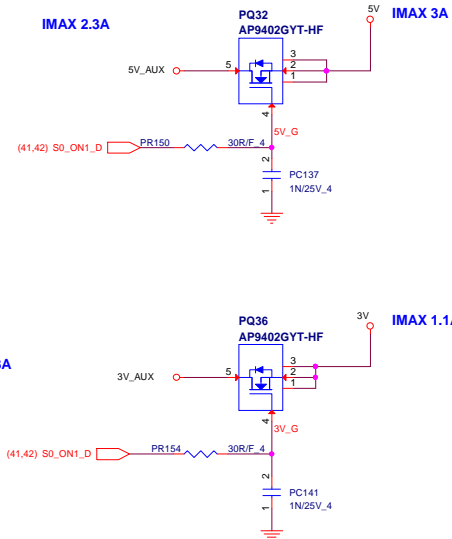
**CONFIDENTIAL**

Load Switch

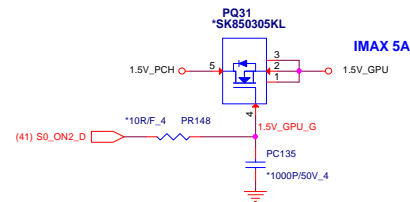
S3 ON Load SW



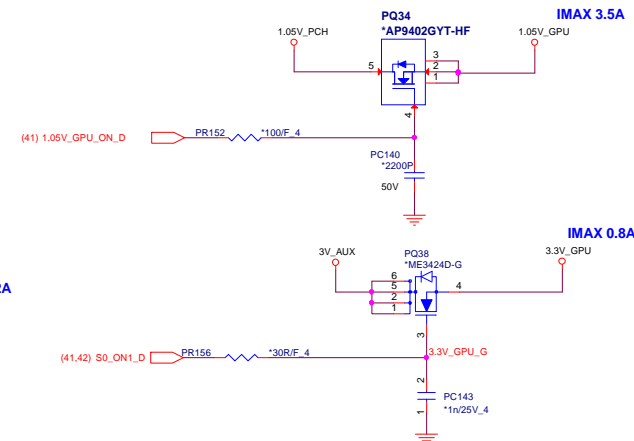
S0 ON_1 Load SW



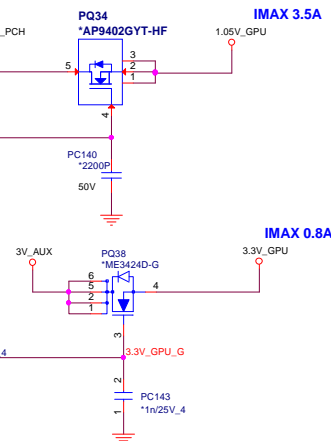
S0 ON_1 Load SW



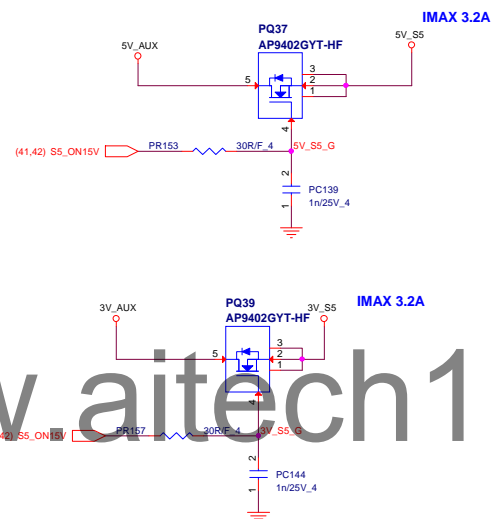
GPU ON_1 Load SW



GPU ON_2 Load SW



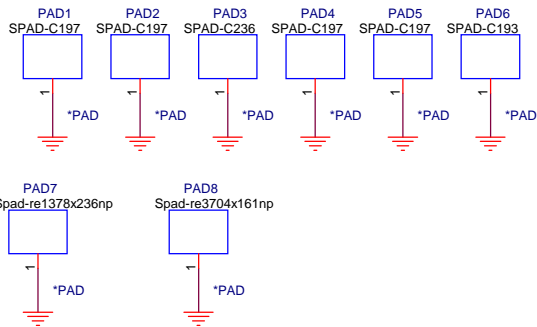
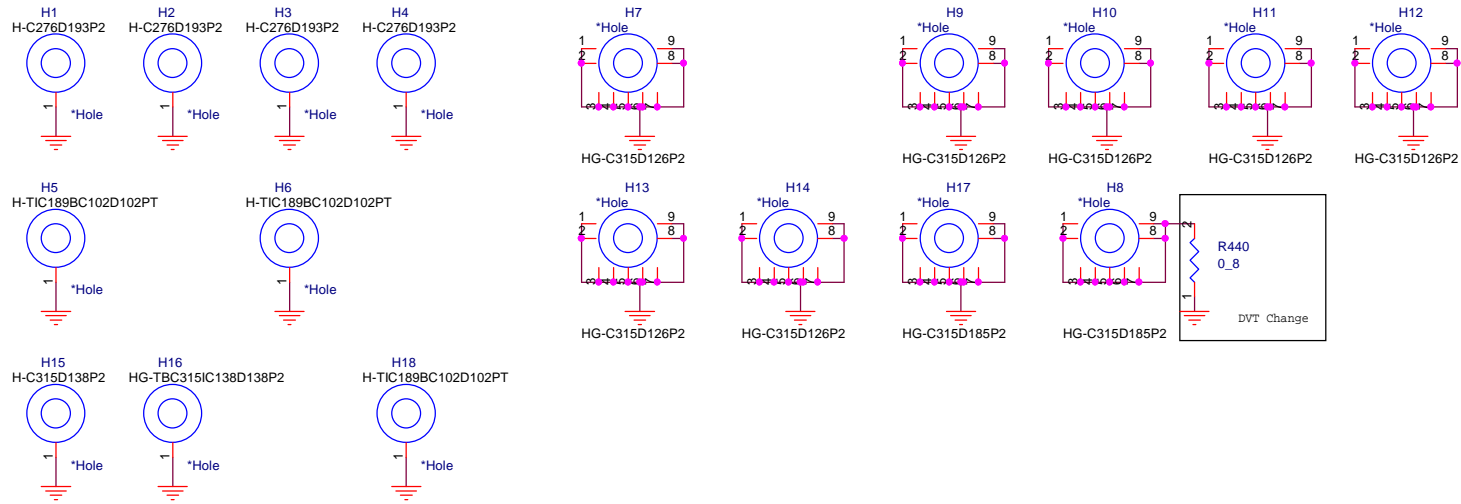
S5 ON Load SW



Mosfet parameter

Mosfet	Package	ID(Ta=25C)	Rds_on_max	Vgs_max
ME3424D-G	TSOP-6	5.0A/6.7A	42m	+/- 20V
AP9402GYT-HF	3x3	11.5A	30m	+/- 20V
SK850305KL	SO-8	22A	14m	+/- 20V

www.aitech1.ru



www.aitech1.ru

EE Portion	Power Portion
DVT-01 Change Board Rev. table and Use R97 to identify we use DVI channel or eDP channel	DVT-27 Add PR23 to 100K ohm for power good
DVT-02 Change R141, R145 to 330 ohms to increase I2C CLK/DATA slew rate	DVT-28 Change PR25 from 0ohm to 100Kohm for limit current
DVT-03 Add Q39, Q40, R277, R278 and R10405 to increase NFC I2C Interface	DVT-29 Add PR58 to 110ohm for meet Haswell SVID spec
DVT-04 Change BT1 P/N because customer request	DVT-30 Change PR54 from 34.8K to 49.9Kohm for change operate frequency
DVT-05 Add R272, R276 and change E1 to 10PIN, because add SPI_I02/3 to increase the R/W speed	DVT-31 Change PC32 from 390PF to 330PF for change compensate
DVT-06 Add R541, R431 pull high resistor on A_I2C-SCL/SDA to fix I2C no pull high issue	DVT-32 Add PQ9 for thermal improve
DVT-07 Add R411 pull down resistor on DVI_HPD signal to fix white screen issue in S3 long run test	DVT-33 Add PQ13 for thermal improve
DVT-08 Change R273 to 0 ohm, because there is a bead before +3.3V_AVDD	DVT-34 Change PC46-47 output voltage from 2.5V down 2V
DVT-09 SWAP CN5.12/14 & CN5.18/20 for layout issue	DVT-35 Change PC55-56 output voltage from 2.5V down 2V
DVT-10 Delete A04 to fix sub-woofer no sound issue	DVT-36 Add smart ID schematic
DVT-11 Add L39-43, L44-53 to fix LVDS EMI Issue	DVT-37 Change throttling schematic
DVT-12 Change R425, R426, R428, R429, R431,R432, R434, R435 footprint from 0402 to 0603 to fix surge issue	DVT-38 Add bead core PL24 & PL25 for PU2
DVT-13 Change R414 to 1K ohm, for Realtek suggestion	DVT-39 Add cap PC72 & PC73 for PU2
DVT-14 Add CN12.5/6/7 to add NPC I2C interface	DVT-40 Add PQ circuit PR450 & PR453 for 1.05V_PCH
DVT-15 Change power button connector CN13 for ME request	DVT-41 Change PR455 from 34K to 34.8Kohm for OCP
DVT-16 Reserve ADB/9 for ESD team request	DVT-42 Change PR452 from 4.87K to 4.9Kohm for Vo improve
DVT-17 Connector EC_SCK_R to GND via EC1 for EMI team request	DVT-43 Add PQ circuit PR456 & PR458 for 1.2V
DVT-18 Connect RTC_VCC to GND Via C408	DVT-44 Remove 12V schematic
DVT-19 Add a GPO 1.05V_GPU_ON to meet GPU Power sequence	DVT-45 Change PC100-101 output voltage from 2.5V down 2V
DVT-20 Connect U26.3 to RTC_VCC to fix single net issue	DVT-46 Change PC117 & PC120 output voltage from 2.5V down 2V and PC121 pop
DVT-21 Add C325 for USB Dongle power	DVT-47 Change PR127 & PC123 footprint and pop for EMI request
DVT-22 Use a switch IC to generate the USB dongle power	DVT-48 Change PR143 & PC134 footprint and pop for EMI request
DVT-23 Use a switch IC to generate the USB2 power	DVT-49 Add PQ circuit PR459 & PR460 for VGA_CORE
DVT-24 HWPL 3.5V connect to EC directly to meet RSMRST# power off sequence	DVT-50 PR439 change pop for PG signal
DVT-25 Change mSATA pin define to meet mini PCI-E spec	DVT-51 Change PR443 from 22.6K to 23.7Kohm for Vo improve
DVT-26 Connect 5V_S5 to U28.2/3, and S3_ON to U28.4 to fix USB3 leakage issue.	DVT-52 PR133 & PC48 change pop for EMI request
	DVT-53 Add discharge circuit for 1.5V_GPU
	DVT-54 Add circuit to meet GPU power sequence
	DVT-55 PQ34 change 3x3 package for current rating
	DVT-56 PQ37 change 3x3 package for current rating
	DVT-57 PQ39 change 3x3 package for current rating
	DVT-58 AC81 change 1UF 25V for ROHS

PVT Portion	PVT2 Portion
PVT-01 Change board Revision to PVT1	PVT2-01 Change board Revision
PVT-02 Exchange SATA & mSATA port as customer request	PVT2-02 Change to 820 ohms that tune I2C falling time
PVT-03 Change R102 VDD to 3V, and reserve 3V_S5 to modify Clear CMOS to power on issue	PVT2-03 FAB request, improve overshoot
PVT-04 Change E1 to 10pin as customer request	PVT2-04 change to 3V that prevent U36 from damage
PVT-05 pull up GP1027, GP1031 GP1072, and PCH_wake# to VCCDOW to support Deep Sx	PVT2-05 AR62,67,75,77 change 93.1Kohm improve AMP gain
PVT-06 Change VCCDOW from 3V and reserve 3V_S5 to modify clear CMOS to power on issue	PVT2-06 AL11,14,17,18 change 1uH improve high frequency and
PVT-07 Add A54, A55, A56 to increase discharge speed to modify Clear CMOS to power on issue	AC68,75,96,100 change 1000PF improve high frequency
PVT-08 Change U1 footprint because of old part will be KOL	PVT2-07 AC82-85 change rating voltage
PVT-09 Change U7 P/N to separate VBIOS rom from scalar firmware rom	PVT2-08 Add AC64,69,70,71 improve white noise
PVT-10 Delete CN51 because of old part will be KOL	PVT2-09 CN15.33, CN15.35 change to Card_3V3 and
PVT-11 Change Y4 footprint because of old part will be KOL	CN15.39 change to GND to prevent assembly issue
PVT-12 Change R128 to short pad	PVT2-10 PR83 & PR84 from 47K to 4.7Kohm can improve PU19 pin3 voltage drop
PVT-13 R128 change to short pad	And Add PC77 0.1uF can improve PU19 pin3 voltage drop
PVT-14 R128 change to short pad	PVT2-11 4. PR151 from 560 to 490ohm improve LED brightness
PVT-15 R125, R127 change to short pad	PVT2-12 Add PC78 0.1uF decay Vin noise
PVT-16 R152, R154 change to short pad	PVT2-13 change to 0603 size because of lack of material
PVT-17 R161 change to short pad	PVT2-14 Add PR93 & PR94 for judge adapter ID
PVT-18 Change NPC select pin to EC	PVT2-15 Add AD_ID pin for judge adapter ID
PVT-19 R198, R199 Change to short pad	PVT2-16 change USB3 Re-driver to PTN36242LBS
PVT-20 R206 change to short pad	because if use 8723, when eject USB3 device,
PVT-21 R210 Change to short pad	there will be still a yellow mark in device manager
PVT-22 R220 change to short pad	PVT2-17 Modify GPU VRAM configuration & resistance mapping table
PVT-23 R224 change to short pad	
PVT-24 R424 change to short pad	
PVT-25 R273 change to short pad	
PVT-26 R557, R558 change to short pad	
PVT-27 R544, R545 change to short pad	
PVT-28 Change U14 P/N to separate scalar firmware rom from VBIOS rom	
PVT-29 R546, R547 change to short pad	
PVT-30 Change HEMI Conn to R/A to fix ME issue	
PVT-31 Add PS to meet LPS	
PVT-32 Add D33 to prevent ESD issue	
PVT-33 Add D15 & D27 to prevent U18 from ESD damage	
PVT-34 pop R399 and de-pop U36 to reserve I2CT mode	
PVT-35 pop R10406 and de-pop U37 to reserve I2CT mode	
PVT-36 Reserve I44-I43, & C86 because LVDS signal is from STD5300	
PVT-37 Add a signal (Scalar Mute) to Codec to fix pop noise when change HDMI mode	
PVT-38 Change CN27.9, 10 to floating to prevent power surge damage	
PVT-39 Delete AC71 from vendor comment	
PVT-40 Delete AC95 from vendor comment	
PVT-41 AVDD is controlled by EC to fix AVDD power on sequence	
PVT-42 Add AR32, and change the value of AR39, AR42, & AC49 to increase Gain to 4dB	
PVT-43 Change value of AR60 & AR61 and power source to fix pop noise	
PVT-44 Change C351's size to 0603 to fix surge issue	
PVT-45 Add R598, R441, R596, R597 & C661 to fix surge issue	
PVT-46 Change value of C169 because vendor request	
PVT-47 Add AC_lost signal in EC to fix clear CMOS power on issue	
PVT-48 Change NPC select pin & reset pin signal to EC control	
PVT-49 Change U19 power source to 3V_AUX as customer request	
PVT-50 Change CN11 to right angle type	
PVT-51 Add C18_CMOS signal to back of solution of clear CMOS power on issue	
PVT-52 Add D28 to prevent leakage	
PVT-53 Add D31 as SMT request to prevent ESD damage	
PVT-54 Add P4 to meet LPS	
PVT-55 Add D32 as SMT request	
PVT-56 Change value & footprint size of C361, C466, C350 to fix surge issue	
PVT-57 Change Footprint size of R594 to fix surge issue	
PVT-58 Add choke on USB2 interface to fix BMT issue	
PVT-59 Add a pin to detect there is HSB or HSP's USB3 board	
PVT-60 Delete USB charger 2nd source	
PVT-61 Add D30 as SMT line request	
PVT-62 Change SATA signal to port 0 of PCB as customer request	
PVT-63 Change HSD SATA rom to prevent connector broken easily	
PVT-64 Add D29 as SMT line request	
POWER PORTION	
POWER PORTION is because it is only used for debug	
PVT-67 PR8 change to short pad.	
PVT-68 PR5 change to short pad.	
PVT-69 Delete PR13	
PVT-70 Delete PR12	
PVT-71 PR38 change to short pad.	
PVT-72 PR52 change to short pad.	
PVT-73 PR45 & PR48 change to short pad.	
PVT-74 Change Met-name	
PVT-75 PR194 change to short pad.	
PVT-76 Add R677	
PVT-77 PR88 change 26.7Kohm for 150W adapter ID.	
PVT-78 PR192 change 102Kohm for 150W throttling	
PVT-79 Add schematic for slave AC remove not power on	
PVT-80 PR454 change to short pad.	
PVT-81 PR451 change to short pad.	
PVT-82 PR453 change to short pad.	
PVT-83 Delete PR89	
PVT-84 Delete PR96	
PVT-85 PR456 change to short pad.	
PVT-86 Delete PR152	
PVT-87 Change Met-name from 1.5V_E3_R to 1.5V_E3	
PVT-88 Change Met-name from 1.5V_E3_R to 1.5V_E3	
PVT-89 Change Met-name from 1.5V_E3_R to 1.5V_E3	
PVT-90 PR101 change to short pad.	
PVT-91 PR109 change to short pad.	
PVT-92 PR116 change to short pad.	
PVT-93 PR104 change 1.48Kohm for 1.5V_S3 OCP	
PVT-94 Delete PR124 & PR126	
PVT-95 Change PC122 from GND to R0ND	
PVT-96 PR128 change to short pad.	
PVT-97 PR489 change to short pad.	
PVT-98 PR143 & PR146 change to short pad.	
PVT-99 PR130 change 13Kohm for VGA_CORE OCP	
PVT-100 Delete PR14	
PVT-101 PR438 change to short pad	
PVT-102 PR441 change to short pad	
PVT-103 PR442 change to short pad	
PVT-104 PR455 change 12.4Kohm for 1.05V_PCH OCP	